UNIT-I

Integrated Circuits

Integrated circuit :-

* Now-a-days a common person uses electronics in limited purposes like radio, TV, AC, ... all electronic gadgets in real life.

* But electronics has a great growth in communi-cation, industries, control, computer, ... etc.

* electronics plays major role in industries.

* electronics is nothing but an integrated circuit.

* "IC" is a small size and low cost circuit. It consists of both active and passive components are joined together on a single crystal chip of silicon.

→ passive components like resistors, capacitors & inductors. these does not need of external power supply. which absorbs power & stores in the form of energy.

→ active components like transistors & diodes. these are depends on power source. These are modify & control the electrical signals.

Advantages :-

* Small size of IC and hence increased power density.
* Low cost due to batch processing.
* Increased system reliability due to elimination of soldered joints.
* Improved function performance.
* Matched devices (input impedance at each port is equal to output impedance).

→ Increased operating speeds (Absence of parasitic capacitance)
→ reduction in power consumption.

Applications :-

→ Automobiles → All vehicles like cars, bike, - - -
→ Appliances → TV, watches, juice makers, - - -
→ computers.

classification of Ic's :-

Ic's are classified into 3 types. They are

1. Digital Ic's Ex:- MP, MC, DSP's etc.
2. Analog (or) linear Ic's Ex:- memorys, sensors, power supply etc
3. Mixed signal Ic's Ex:- A/D & D/A converters. etc

Based on above requirement, there are 2 different Ic technologies.

1. Monolithic technology
2. Hybrid technology

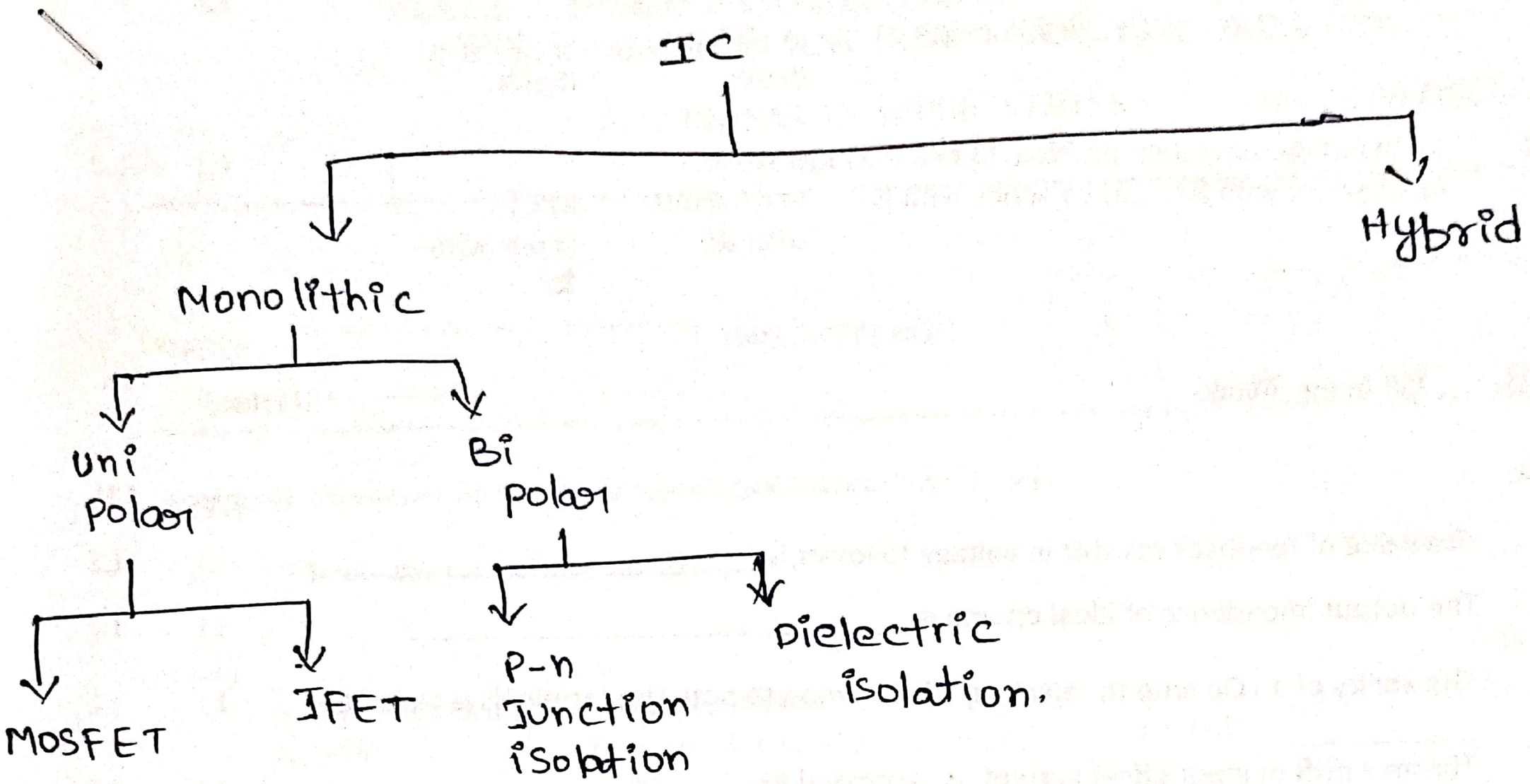
Monolithic :-

All circuit components both active and passive elements & their interconnections are manufactured into (or) on top of a single chip of silicon. These are used, where identical circuits are required. that's why we reduces the cost & more reliable circuits.

Hybrid :-

In this, separate components parts are attached to a substrate and interconnected by using metallization & wire bonds. this is used for custom circuits.

→ Based upon active devices used. Ic's are classified as. ③



IC chip size and circuit complexity :-

→ until 1950's, electronic device technology uses vacuum tube but now-a-days electronics is a result of invention of transistor in 1947.

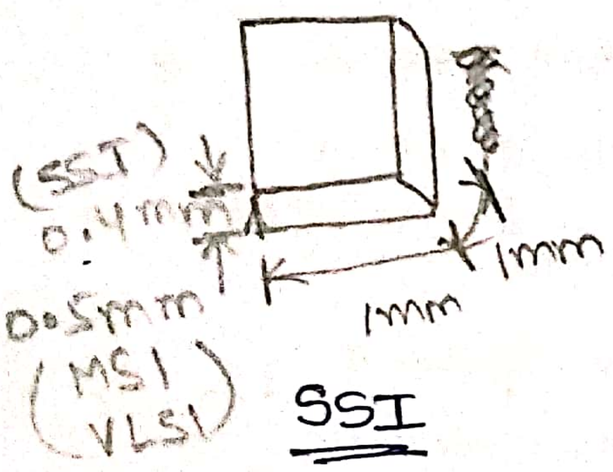
→ the invention of transistor by william B. Schockley, walter H. Brattain & John Bardeen of bell telephone laboratory .. and followed by the developement of IC.

→ The IC was introduced at the beginning of 1960 by both texas instruments & fairchild semiconductors. Invented by Robert Noyce.

→ The size and complexity of IC's have increased rapidly as shown below.

Technology	gates/chip	transistors/chip	Applications	year
1. SSI (Small scale Integration)	3 to 30	100	logic gates flip flops	1960-65
2. MSI (medium scale Integration)	30 to 300	100-1000	Multiplexers counters adders	1965-1970

3. LSI (large scale Integration)	300 to 3000	1000 - 20,000	8-bit MP, ROM RAM	1970-1980
4. VLSI (very large scale integration)	3000 to 30,000	20,000 - 10^6	16 bit & 32 bit MP's	1980-1990
5. ULSI (ultra large scale integration)	more than 30,000	$10^6 - 10^7$	special-processors, smart sensors	1990-2000
6. GSI (Giant Scale integration)	—	$> 10^7$	—	—



chip area

SSI - $1 mm^2$

MSI - $4 mm^2$

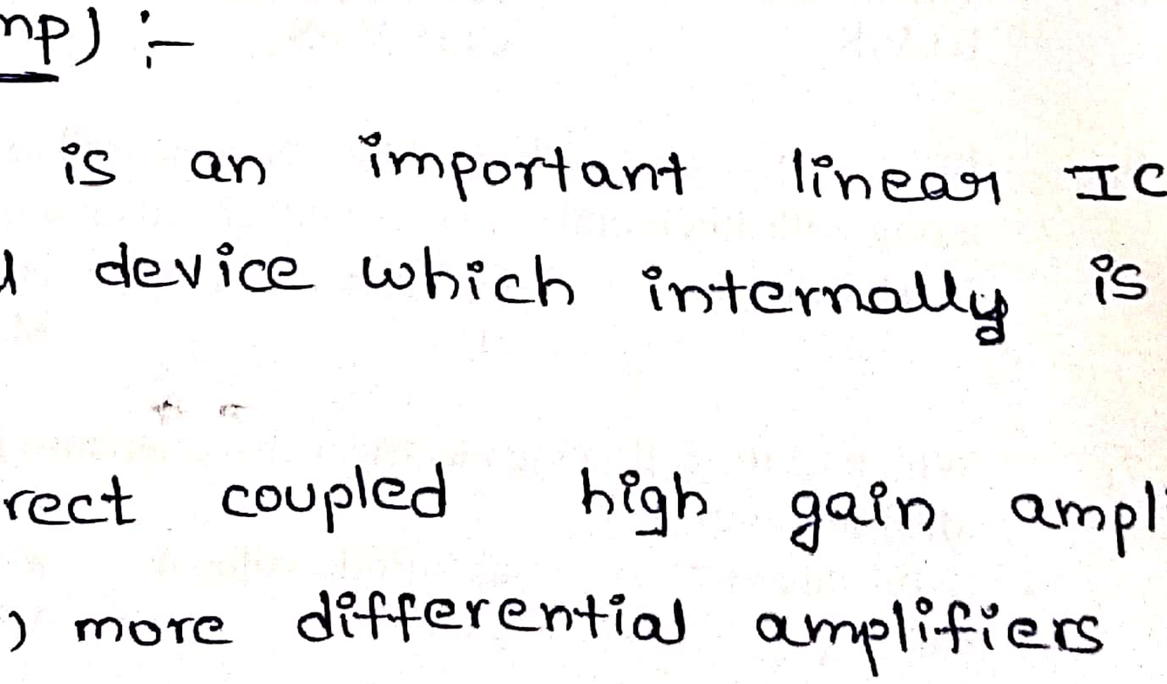
VLSI - $10 mm^2$

operational Amplifier :- (op-Amp) :-

→ operational amplifier is an important linear IC. op-amp is a multi-terminal device which internally is quite complex.

→ op-amp is a direct coupled high gain amplifier usually consisting of one (or) more differential amplifiers ~~and~~ followed by level translator and an o/p stage.

op-amp symbol :-



op-amp consists of 2 i/p terminals (inverting & non-inverting), one o/p terminal and 2 supplies ($+V_{CC}$, $-V_{EE}$).

Def. of op-amp :-

op-amp is an IC that can amplify weak electric signals. the basic role of op-amp is to amplify and o/p the voltage difference between two i/p pins.

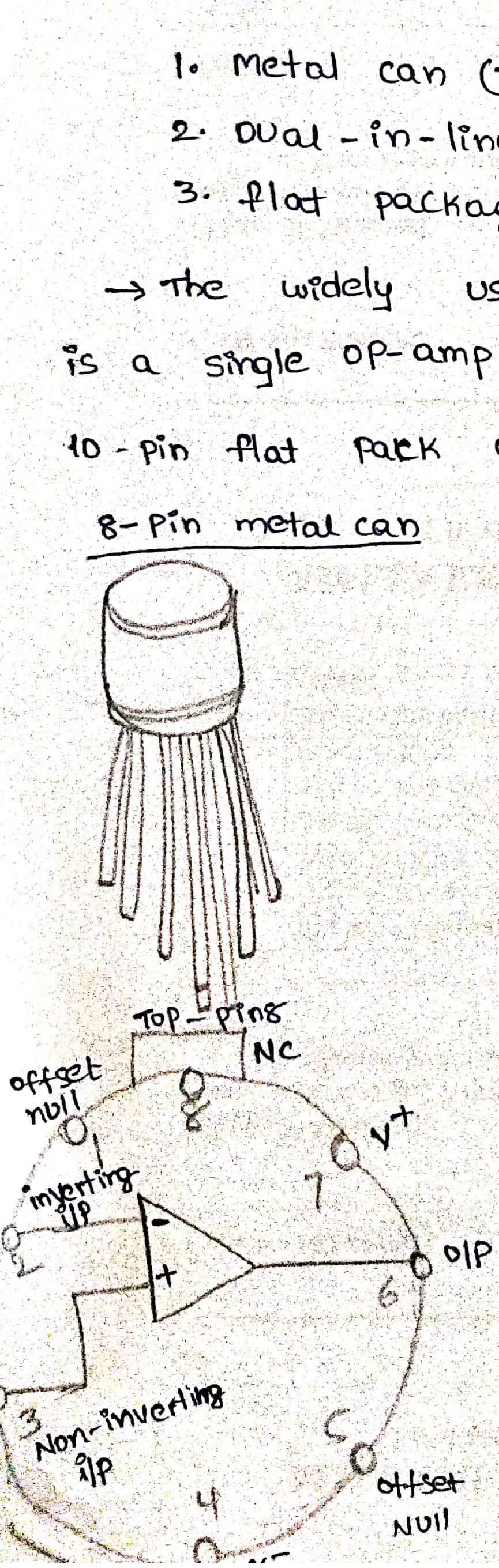
op-amp packages :-

there are mainly three popular packages are available.

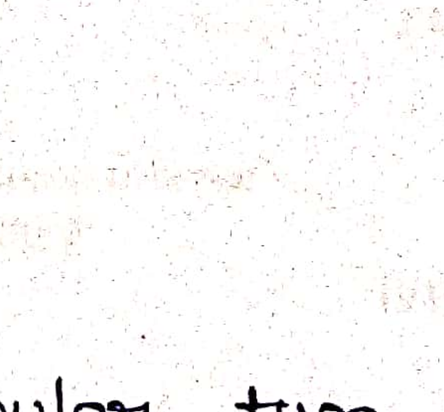
1. Metal can (TO)
2. Dual-in-line (DIP)
3. flat package.

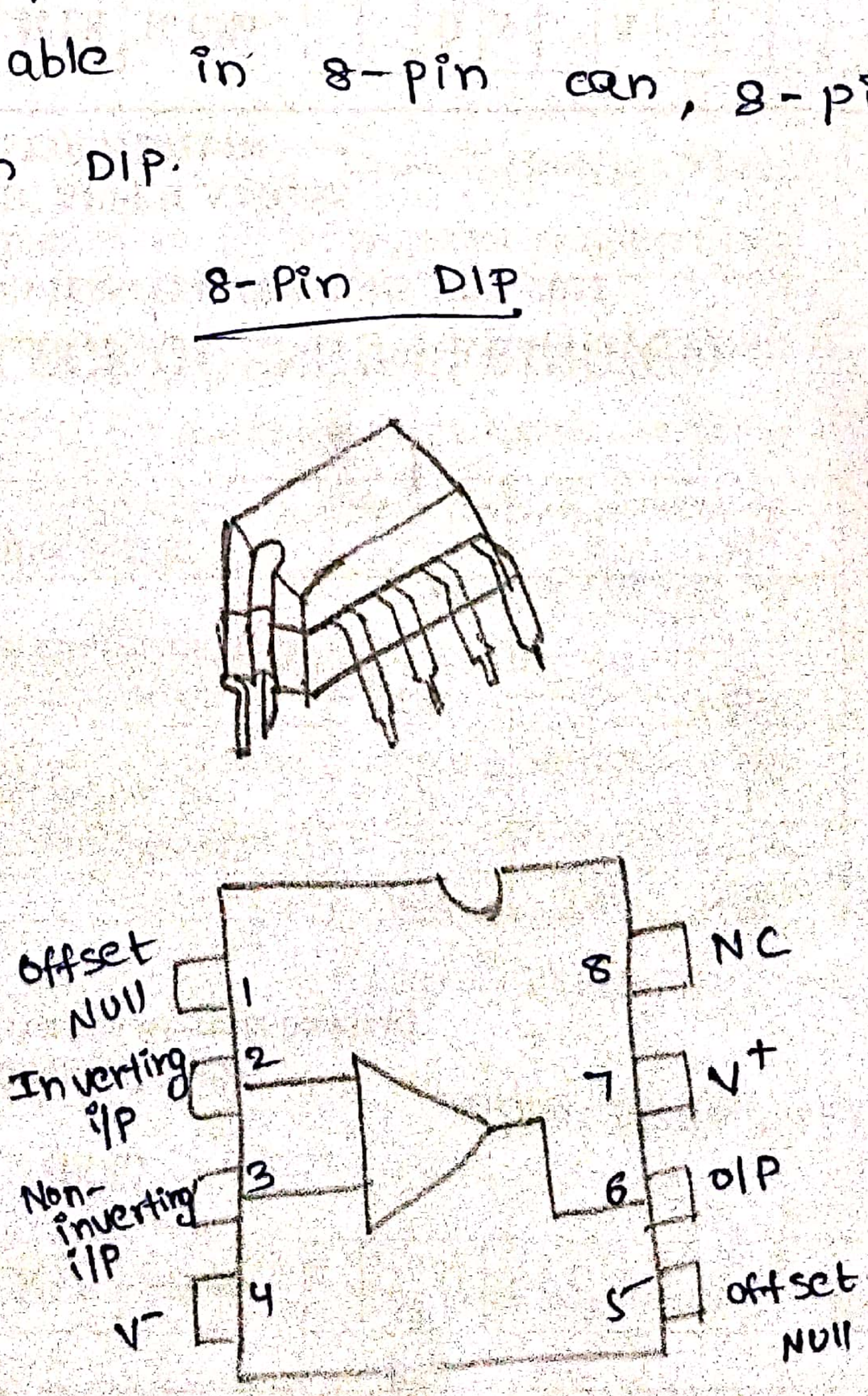
→ the widely used very popular type is µA741. It is a single op-amp & available in 8-pin can, 8-pin DIP, 10-pin flat pack or 14-pin DIP.

8-Pin metal can

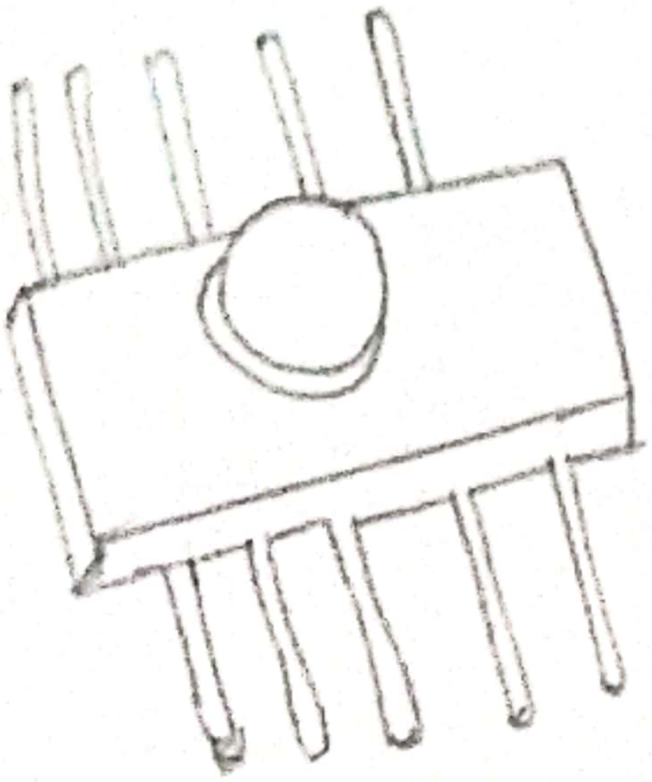


8-Pin DIP

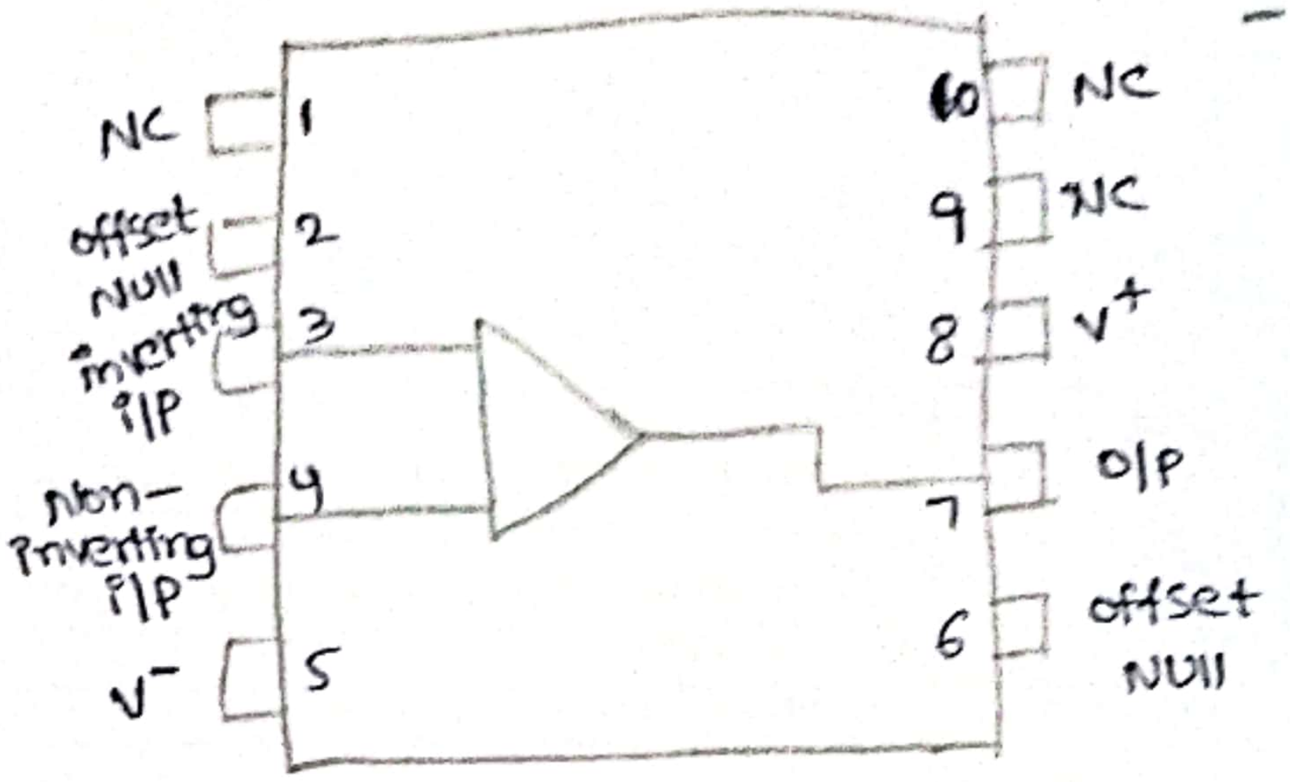




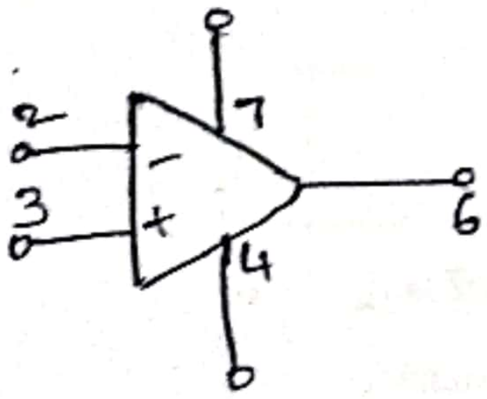
10-pin flat pack

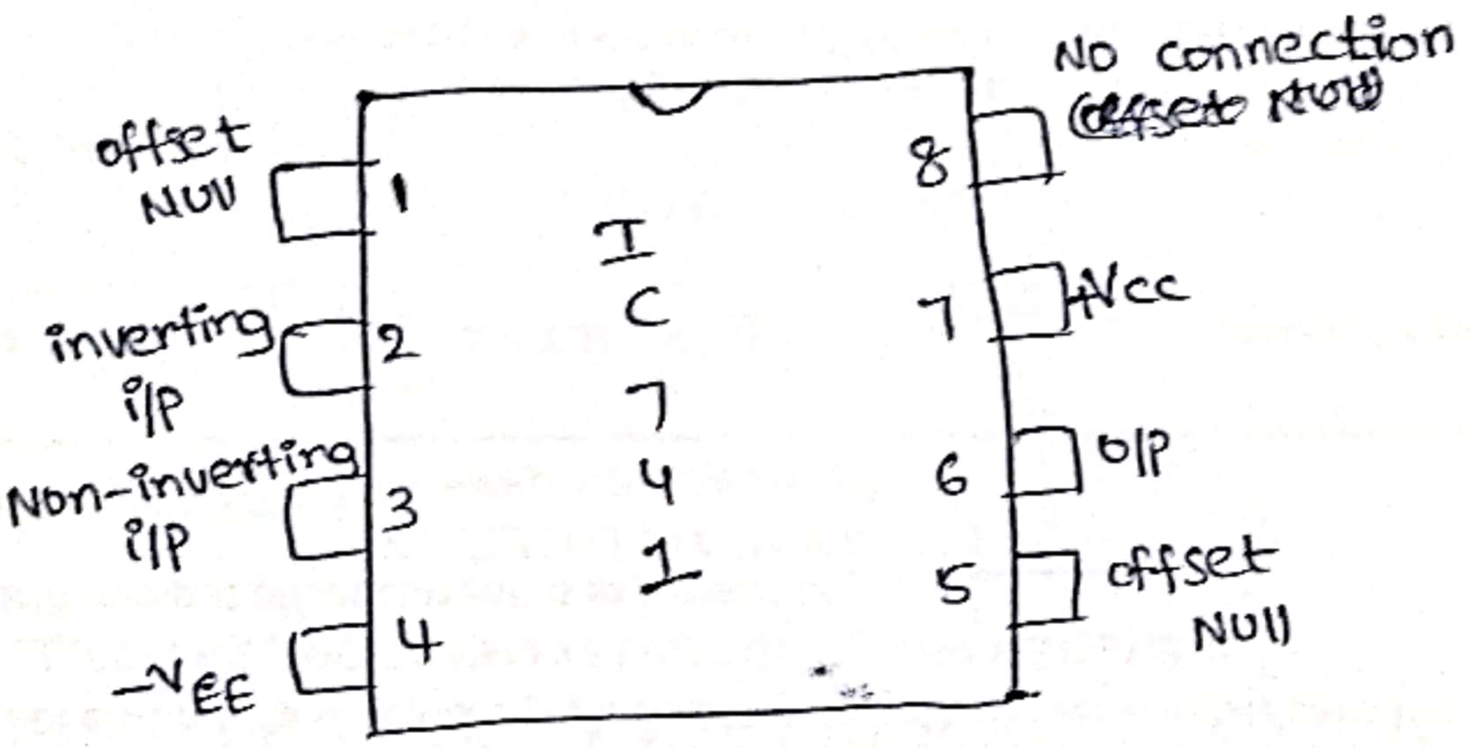


NC → No connection

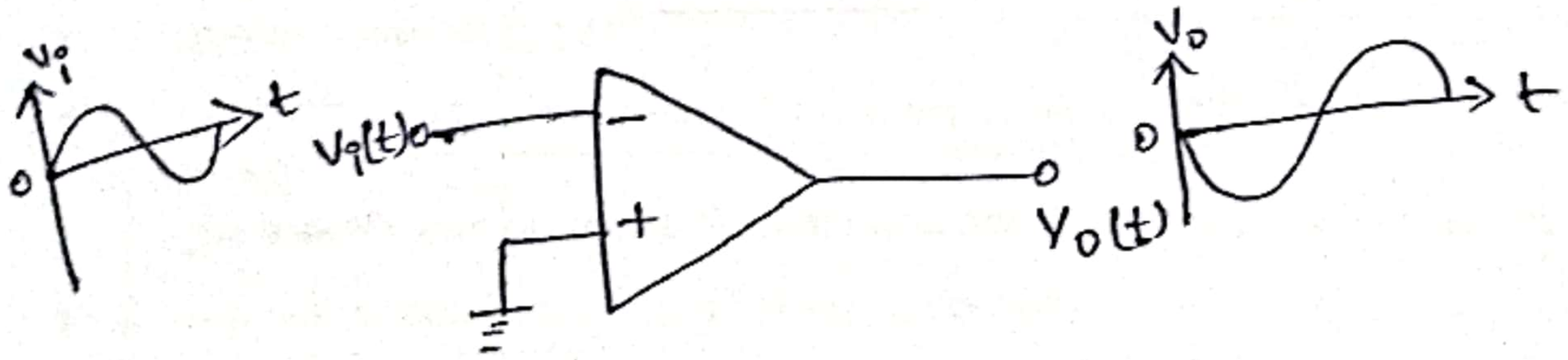


Internal diagram of IC741





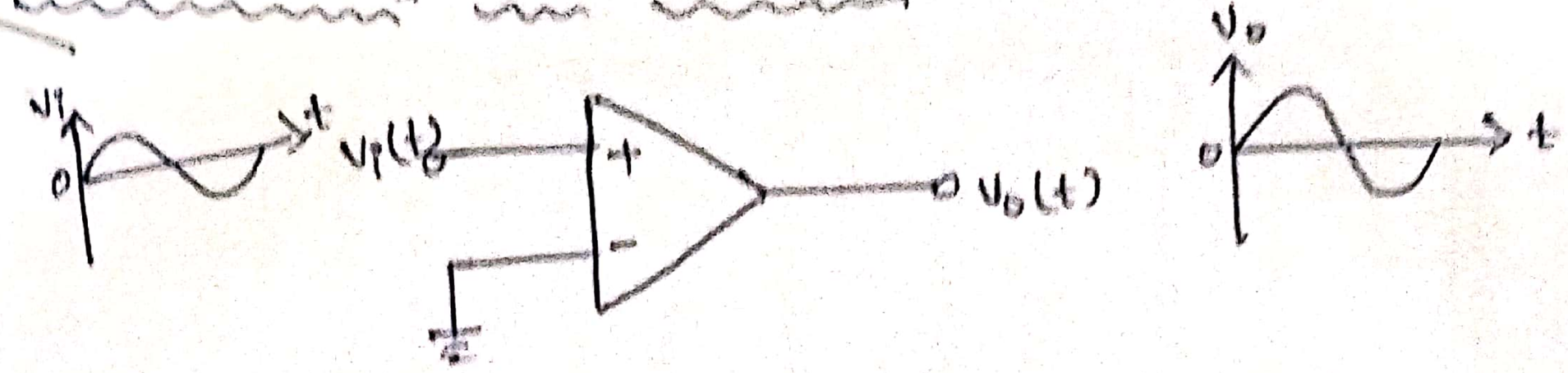
Inverting i/p terminal:-



→ In the above diagram we are applying i/p to the -ve terminal of op-amp & +ve terminal is kept grounded.

→ By observing the $V_i(t)$, $V_o(t)$ signals, it is clear that both are out of phase by 180° for that reason the -ve terminal is called inverting i/p terminal.

Non-Inverting I/P terminal :- (1)



→ In the above diagram we apply I/P signal is given to the +ve terminal & -ve terminal is kept grounded.

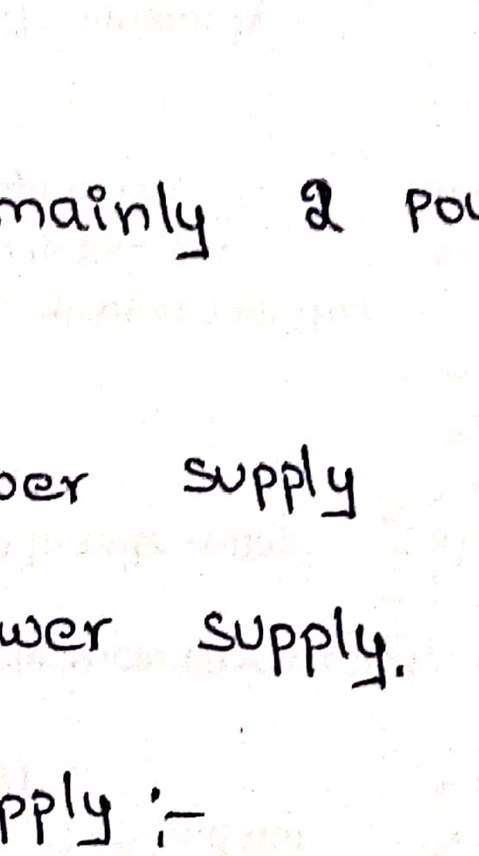
→ By observing $V_i(t)$ & $V_o(t)$ signals, it is clear that both are in phase so +ve terminal is called non-inverting i/p terminal.

Power supply :-

There are mainly 2 power supply connections in op-amp.

1. Balanced Power supply
2. unbalanced power supply.

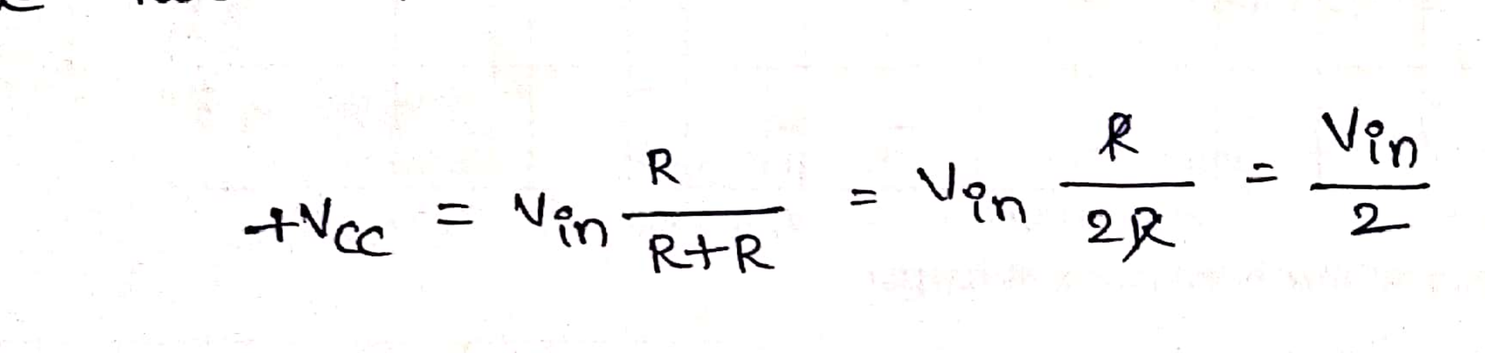
Balanced power supply :-



→ In balanced power supply the two supply voltage magnitude must be equal and the common terminal is kept grounded.

→ In balanced P.Supply, twice the supply voltage will get applied & it may damage the op-amp. Instead of using two power supplies, one can use a single p.s to obtain V^+ & V^-.

Unbalanced Power supply :-



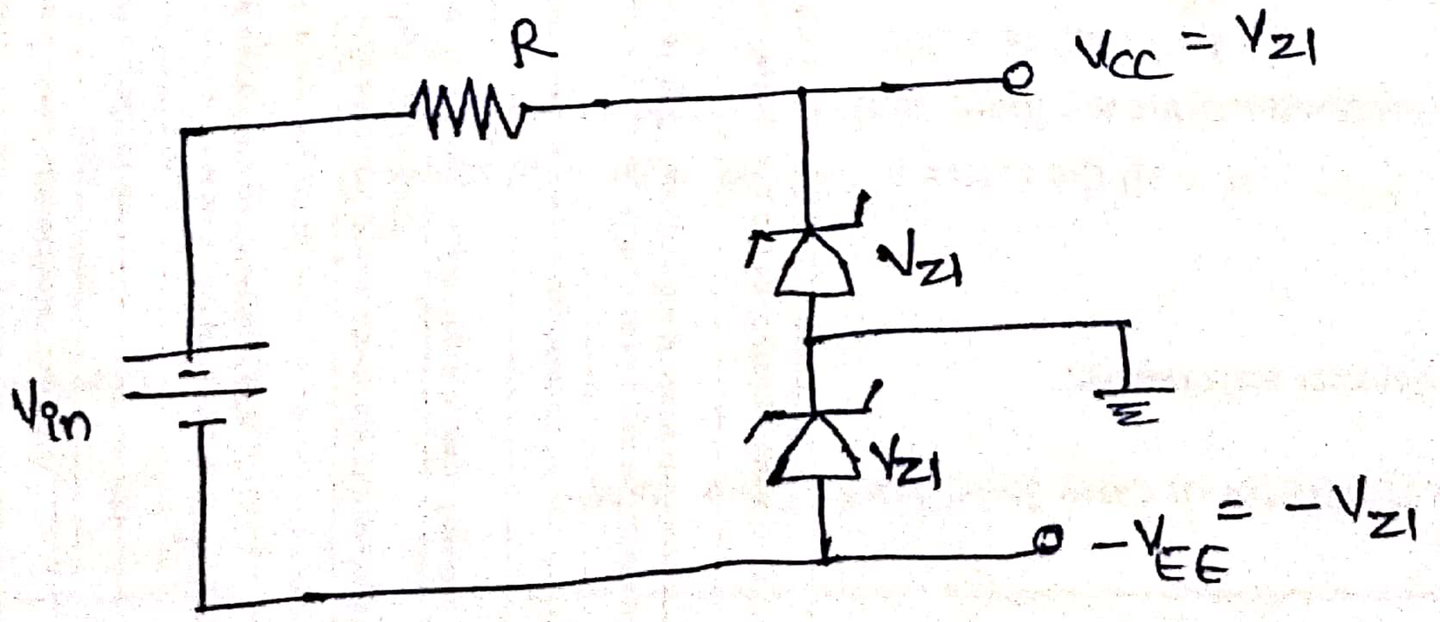
$R > 10K\Omega$

$C = 0.01 - 10\mu F$

→ the two capacitors provide decoupling of the power supply.

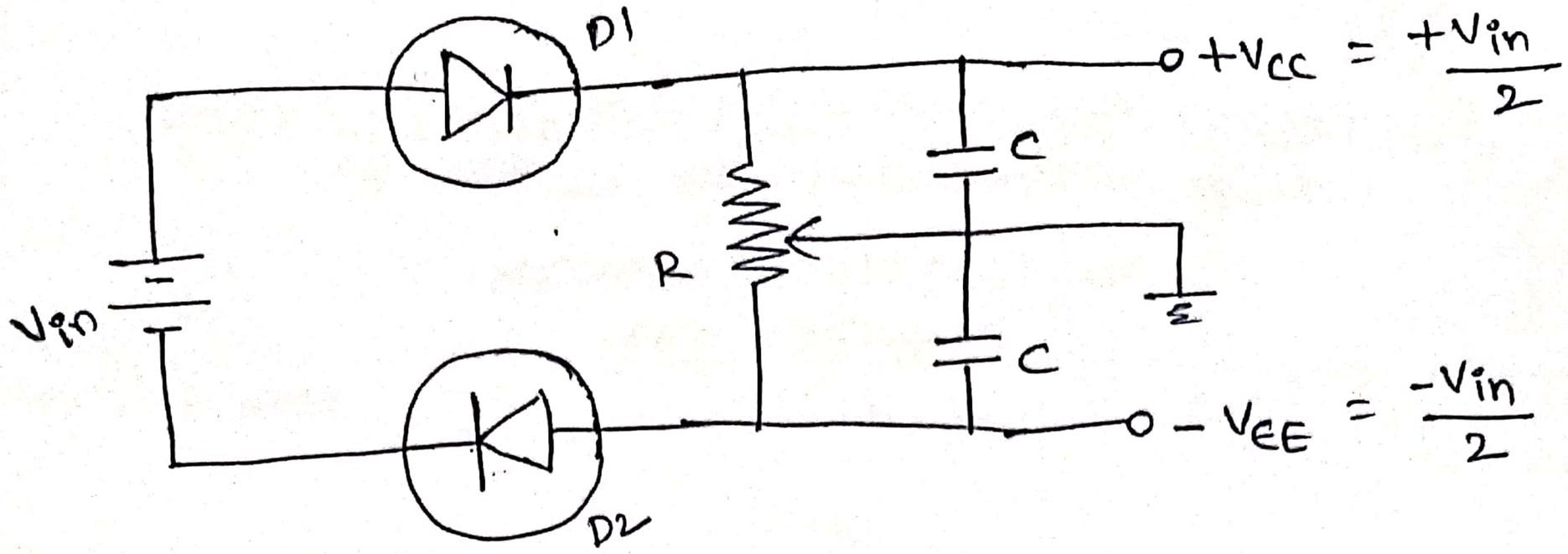
→ $$+V_{CC} = V_{in}\frac{R}{R+R} = V_{in}\frac{R}{2R} = \frac{V_{in}}{2}$$

→ If the voltages required are other than $\frac{V_{in}}{2}$ then above circuit is non preferable then we can use Zener diodes of appropriate voltage rating can be used.



→ Many times practically due to mismatch in the devices equal +ve & -ve voltages are not available, to adjust them a potentiometer can be used as shown below.

→ To avoid the damages due to reversal polarities connected to integrated circuit, the diodes D_1 & D_2 can be used.



Features of 741 op-Amp :-

→ short circuit & overload protection provided

→ large common mode rejection ratio (CMRR) and differential voltage ranges. Ideally CMMR is infinity.

→ No external freq. compensation is required. It also does not need any external compensation for phase component. This simplifies the circuit design and minimize the number of components used.

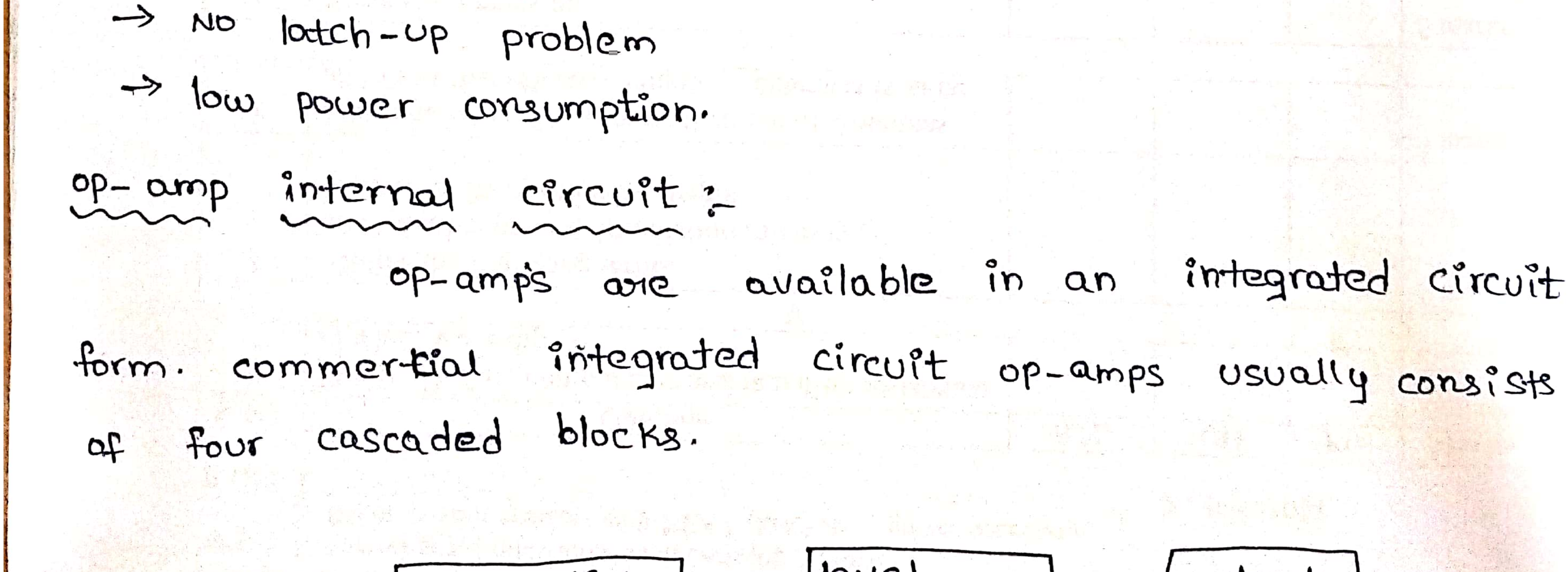
→ offset voltage null capability

→ No latch-up problem

→ low power consumption.

op-amp internal circuit :-

op-amp's are available in an integrated circuit form. commertial integrated circuit op-amps usually consists of four cascaded blocks.



Input stage :-

→ the input stage requires "high input impedance" to avoid loading on the sources. It requires two input terminals. It also requires low o/p impedance.

→ All such requirements are achieved by using dual i/p balanced o/p differential amplifier as the i/p stage

→ the function of differential amplifier is to amplify the difference between the two i/p signals.

→ this stage provides most of the voltage gain of the amplifier.

Intermediate stage :-

→ the o/p of the i/p stage drives the next stage which is an intermediate stage

→ This is another differential amplifier with dual i/p unbalanced (single ended) output.

→ the overall gain requirement of the "op-amp is very high."

level shifting stage :-

→ All the stages are directly coupled to each other. As the op-amp amplifiers, d.c signals are also directly coupled.

→ Because of that the DC level is raises stage by stage such a high d.c voltage level may drive the transistors into saturation.

→ this may cause distortion in the output.

→ Hence before the o/p stage, it is necessary to bring such a high dc voltage level to zero volts w.r.t. ground.

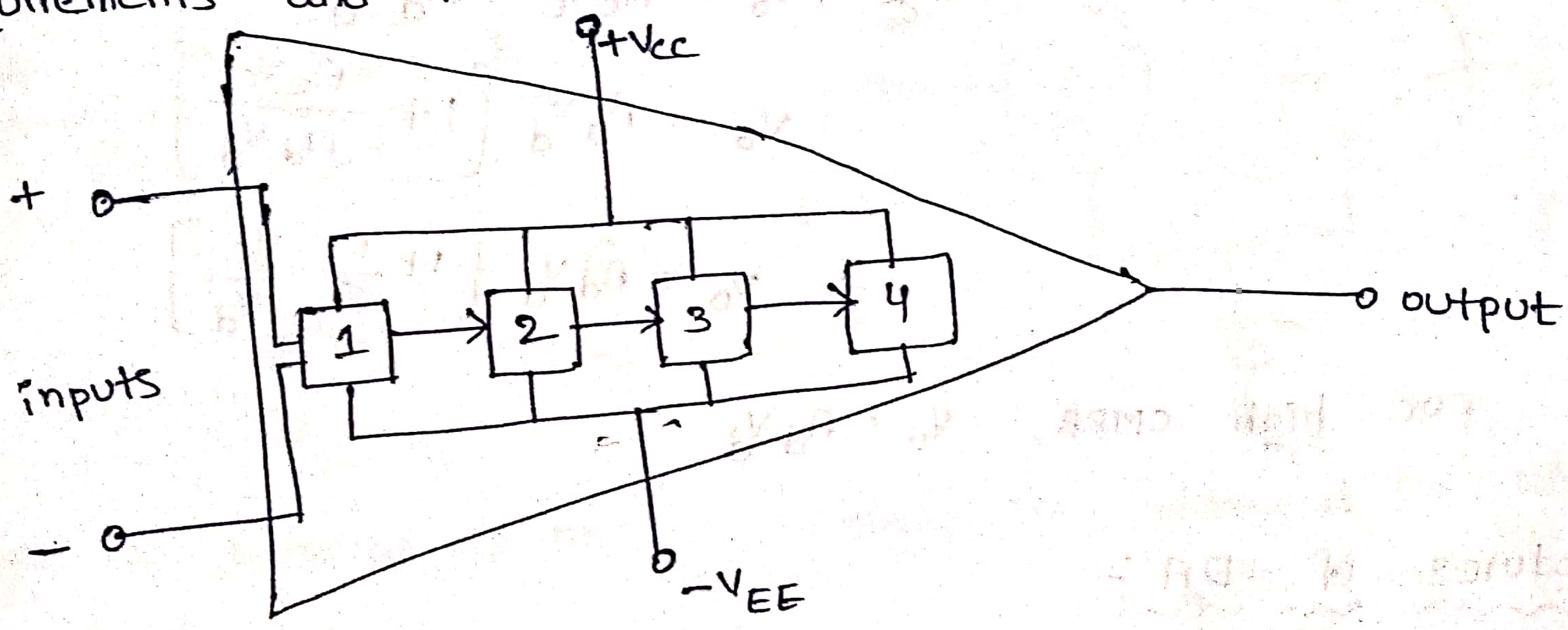
→ the level shifter stage brings the d.c level down to ground potential, when no signal is applied at the i/p terminals.

output stage :-

→ The basic requirements of an output stage are

* low output impedance
* large AC
* output voltage swing
* high current sourcing & sinking capability

→ The push pull complementary amplifier meets all these requirements and hence used as an o/p stage.



Differential Amplifier :-

→ It is the basic building block of op-amp.

→ It amplifies the difference between two input voltage signals and rejects the common-mode signals, Hence it is called as differential amplifier.

common-mode Rejection Ratio (CMRR) :-

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common-mode rejection ratio.

→ CMRR is defined as the ratio of the differential voltage gain, A_d to common mode voltage gain, A_c.

$$CMRR = \rho = \left| \frac{A_d}{A_c} \right|$$

→ For ideal DA, $A_c = 0$ then CMRR is infinite.

→ For practical DA, A_d is large, A_c is small hence CMRR is very large.

$$\text{CMRR in dB} = 20 \log \left| \frac{A_d}{A_c} \right| \text{ dB}$$

→ the output voltage, $V_o = A_c V_c + A_d V_d$

$$V_o = A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{\rho} \cdot \frac{V_c}{V_d} \right]$$

For high CMRR, $V_o = A_d V_d$

Features of DA :-

* High differential voltage gain
* low common mode gain
* High CMRR
* High i/p impedance
* low o/p impedance
* large bandwidth

Types of Differential Amplifiers :-

There are 4 types of DA's.

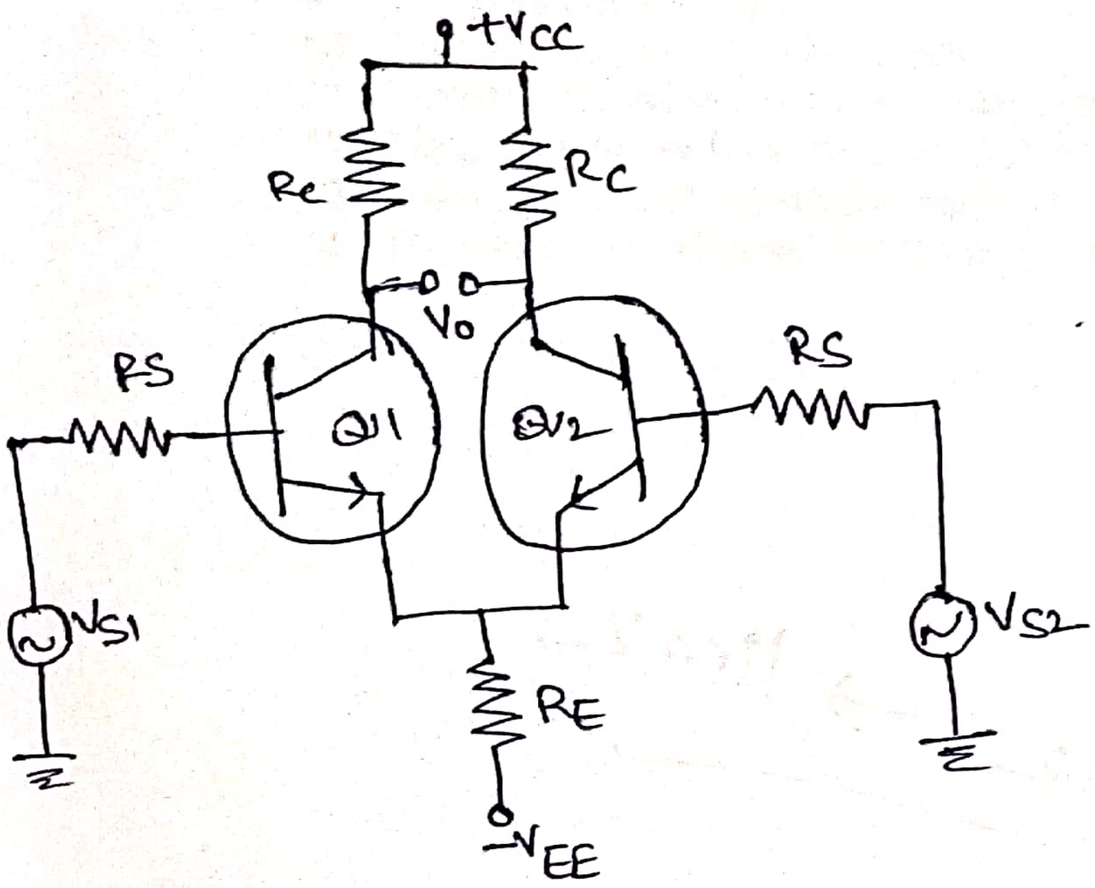
1. Dual i/p balanced o/p DA
2. Dual i/p unbalanced o/p DA
3. single i/p balanced o/p DA
4. single i/p Unbalanced o/p DA.

→ If the o/p is taken between the two collector terminals, it is called balanced o/p (or) double ended o/p.

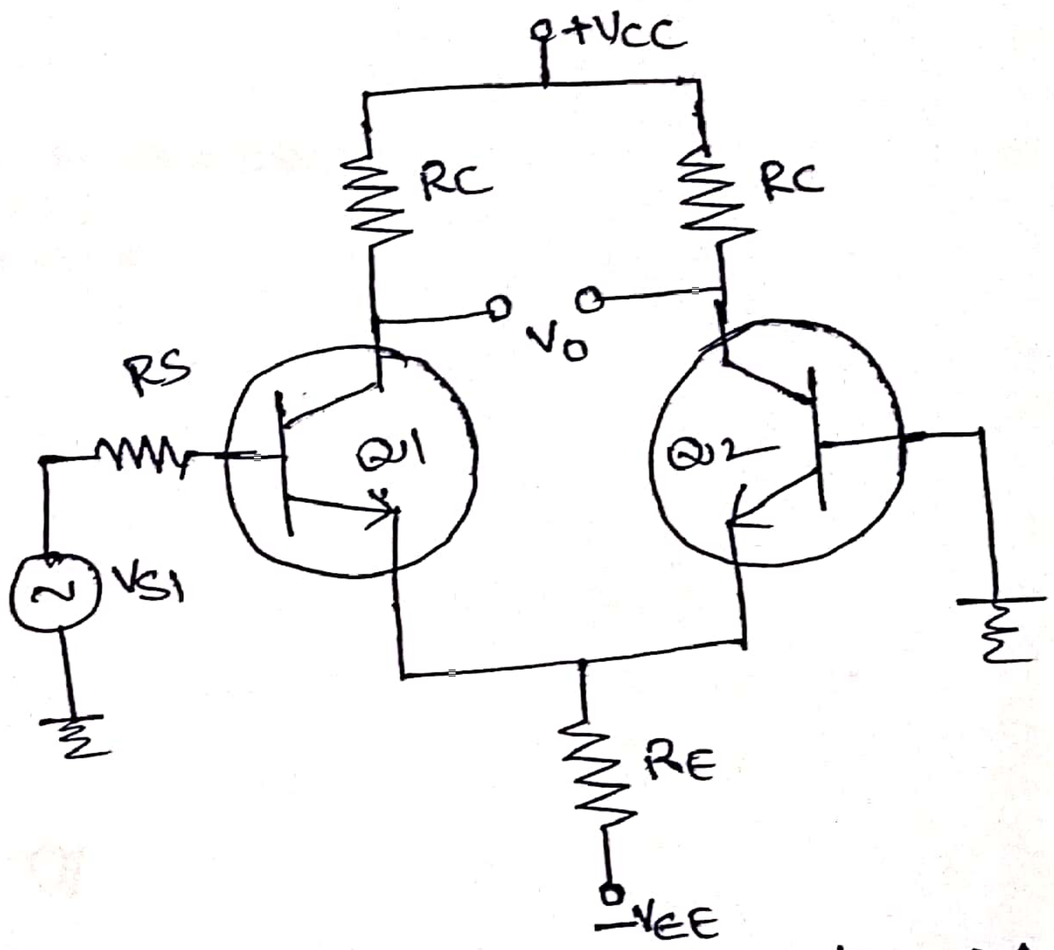
→ If the o/p is taken between one collector w.r.t. ground, it is called unbalanced o/p (or) single ended o/p.

→ If the signal is given to both the i/p terminals, it is called as dual i/p.

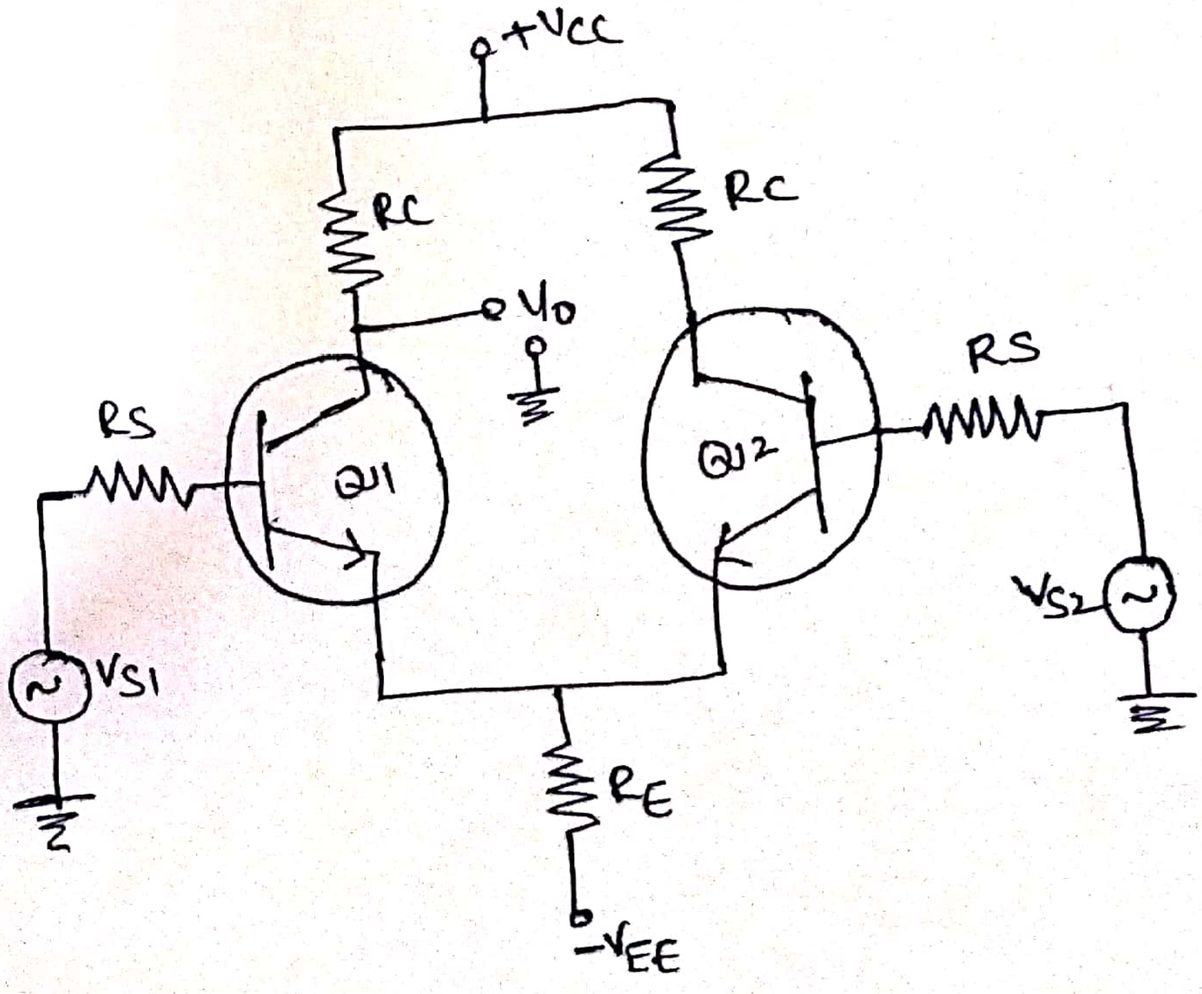
→ If the signal is given to only one i/p terminals and other terminal is grounded, is called single i/p (or) single ended i/p.



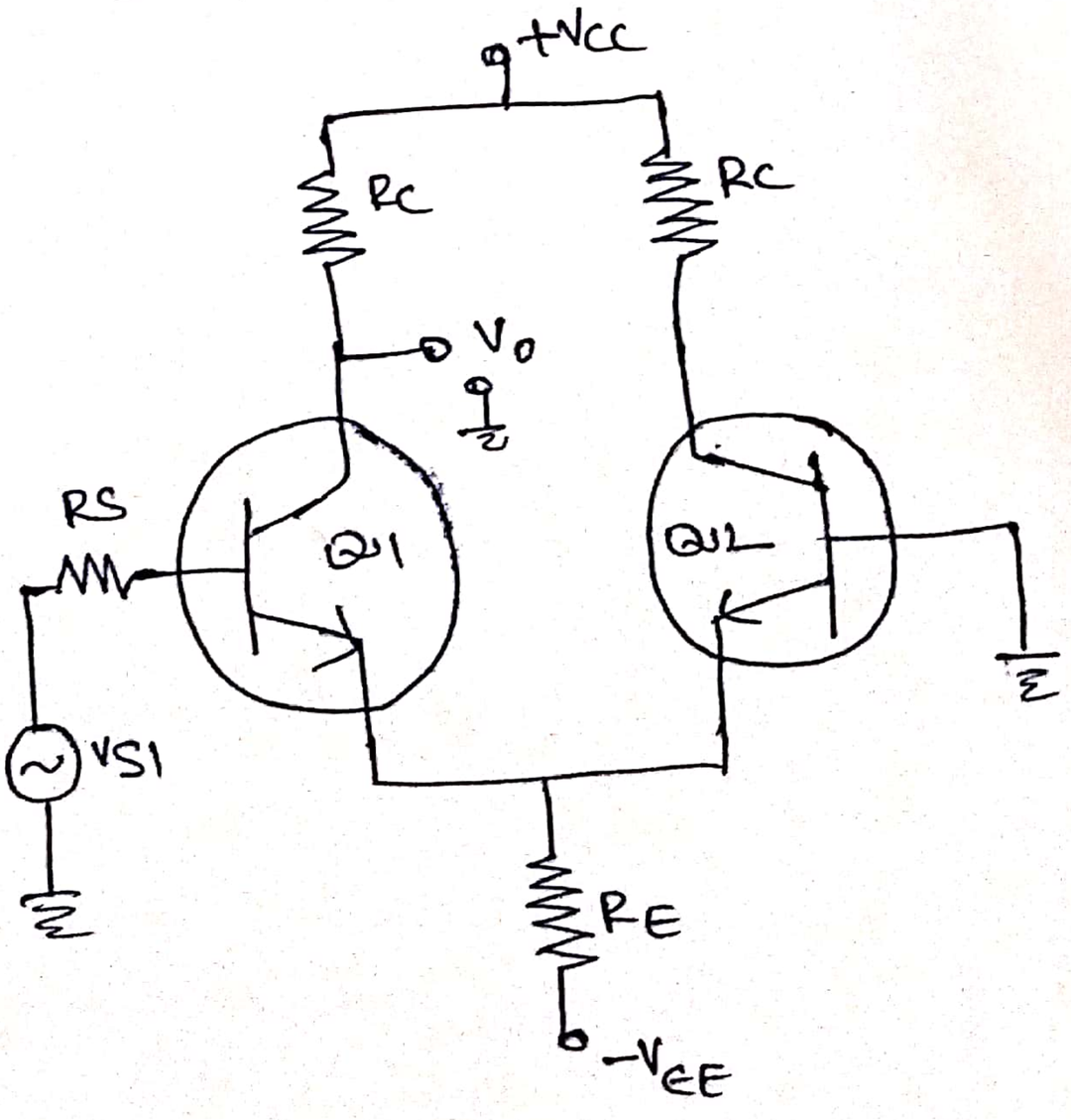
Dual i/p balanced o/p DA



Single i/p balanced o/p DA.



Dual i/p unbalanced o/p DA



Single i/p unbalance o/p DA.

Formulae :-

1. Difference voltage, $V_d = V_1 - V_2$.

2. Differential output voltage, $V_o = A_d V_d$

3. Differential gain, $A_d = \frac{V_o}{V_d}$ (or) $A_d = \frac{V_1 - V_2}{2}$ (or) $20 \log_{10}\left(\frac{V_o}{V_d}\right)$ (in dB)

4. where A_1 & A_2 are the gains of two signal voltages of V_1 and V_2 respectively.

4. common-mode signal voltage, $V_c = \frac{V_1 + V_2}{2}$

5. common-mode gain, $A_c = \frac{V_o}{V_c}$ (or) $A_c = A_1 + A_2$ (or) $20 \log_{10} \frac{V_o}{V_c}$ (in dB)

6. output voltage due to common mode signal is $V_o = V_c A_c$

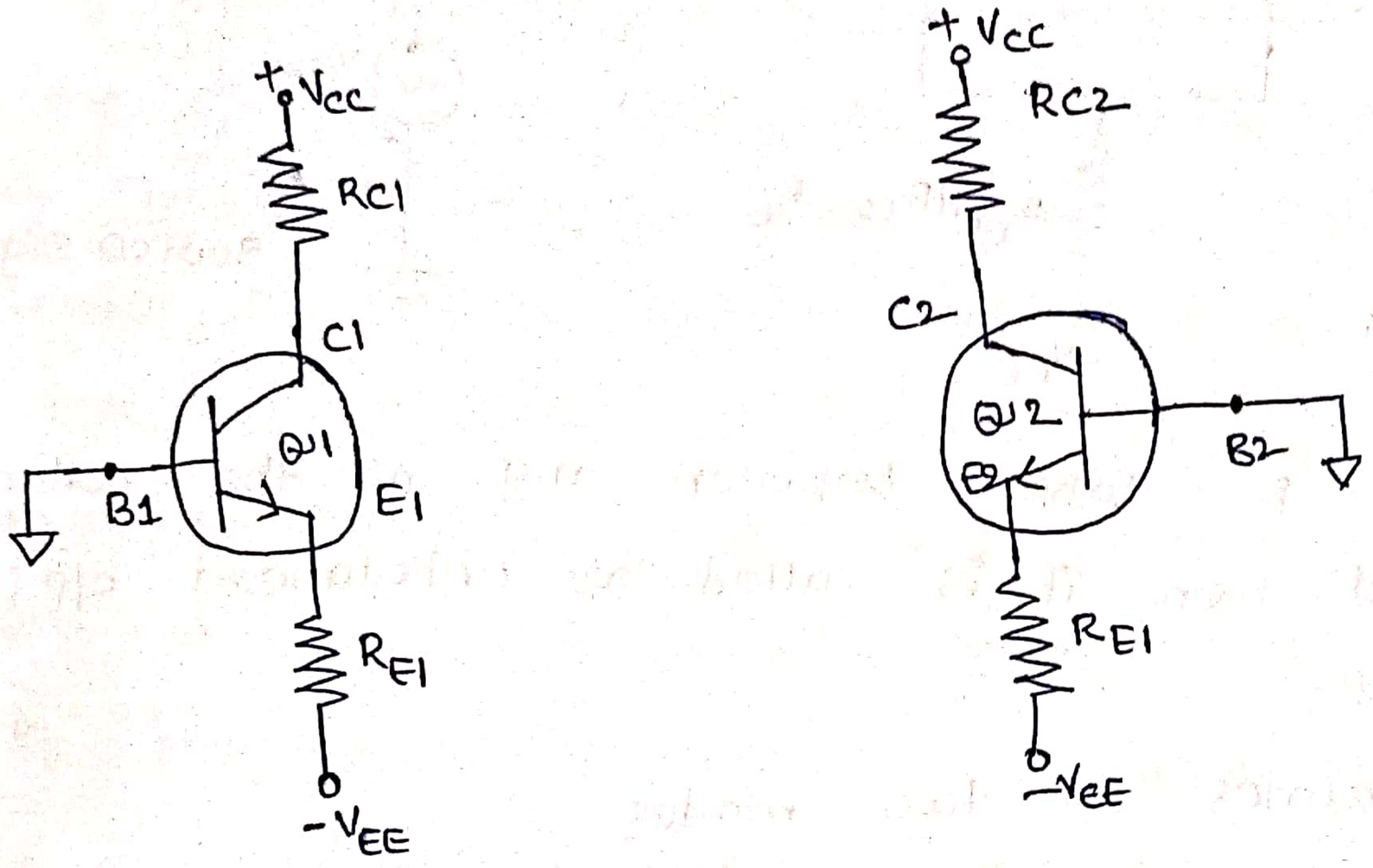
7. Total output voltage for any differential amplifier is

$$V_o = A_d V_d + A_c V_c.$$

Dual i/p balanced o/p differential amplifier :-

This is also known as emitter coupled differential amplifier.

The transistorised differential amplifier basically uses the emitter biased circuits which are shown in fig. below.



→ the two transistors Q1 & Q2 are having exactly matched characteristics.

→ the two collector and emitter resistances R_{C1}, R_{C2}, R_{E1} and R_{E2} are equal.

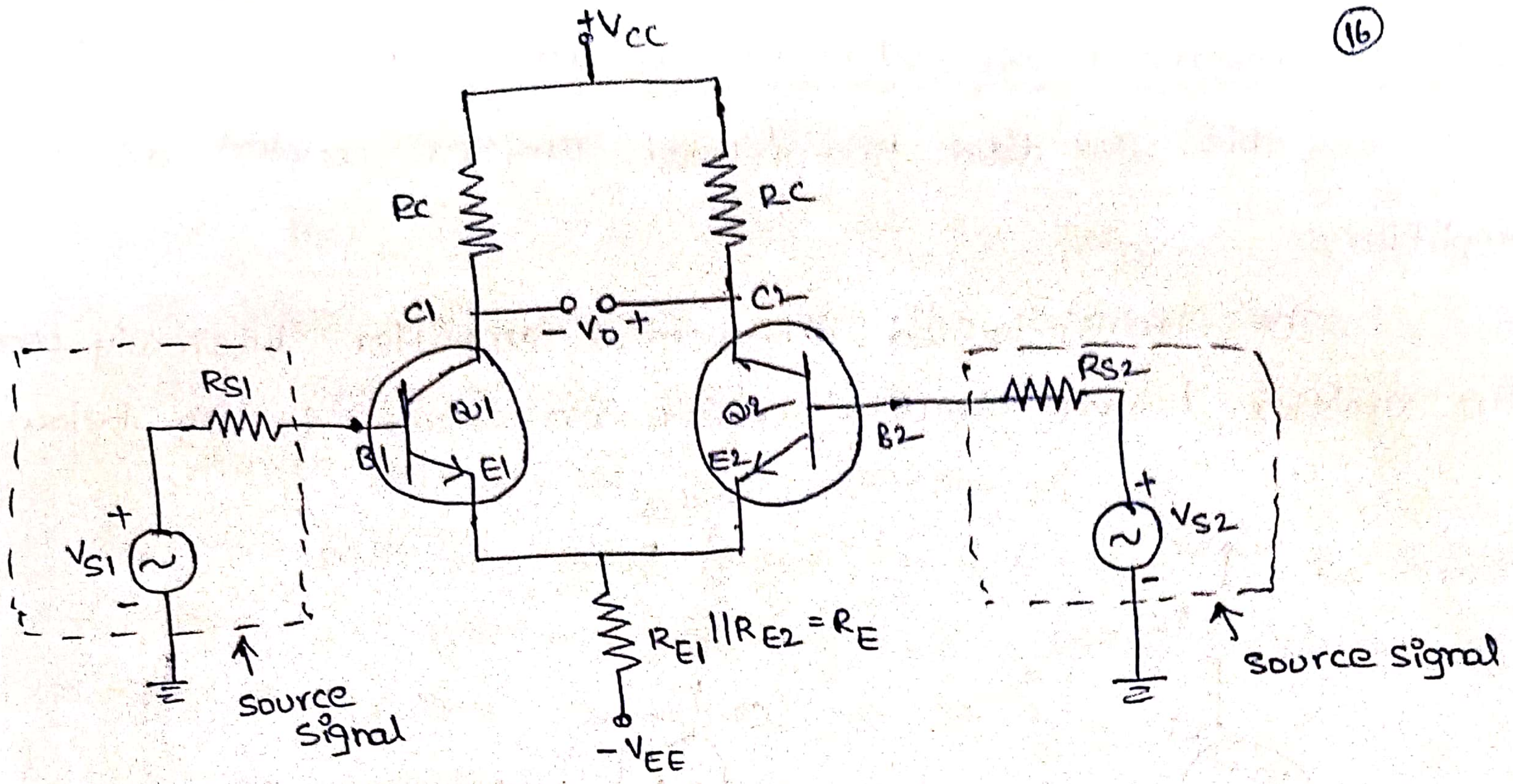
$$R_{C1} = R_{C2} = RC \quad ; \quad R_{E1} = R_{E2} \quad \text{and}$$

$$|V_{CC}| = |-V_{EE}|$$

∴ the magnitudes must be equal

→ the dual i/p balanced o/p DA can be obtained by coupling both emitters of the emitter biased circuits and is shown below fig.

→ If the collector o/p is taken between two collector terminals without any ground, then it is called as balanced o/p (or) double ended o/p (or) floating o/p.



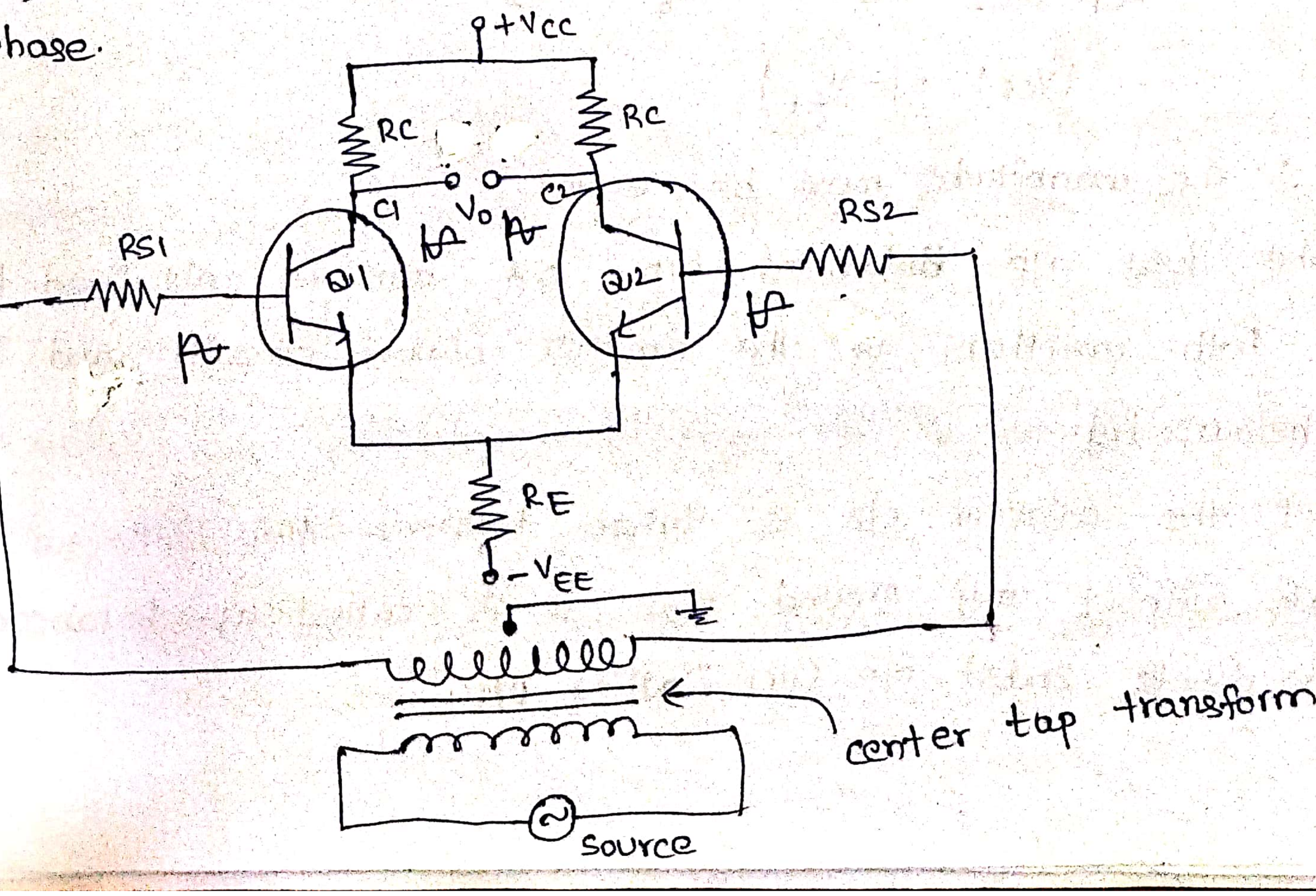
→ when the o/p is taken between any of the collectors and the ground, then it is called as unbalanced o/p (or) single ended o/p.

→ the DA operates in two modes.

1. Differential mode operation
2. common mode operation.

Differential mode operation :-

* Differential mode means $V_{S1} \neq V_{S2}$. consider the two i/p signals which are same in magnitude but 180° out of phase.



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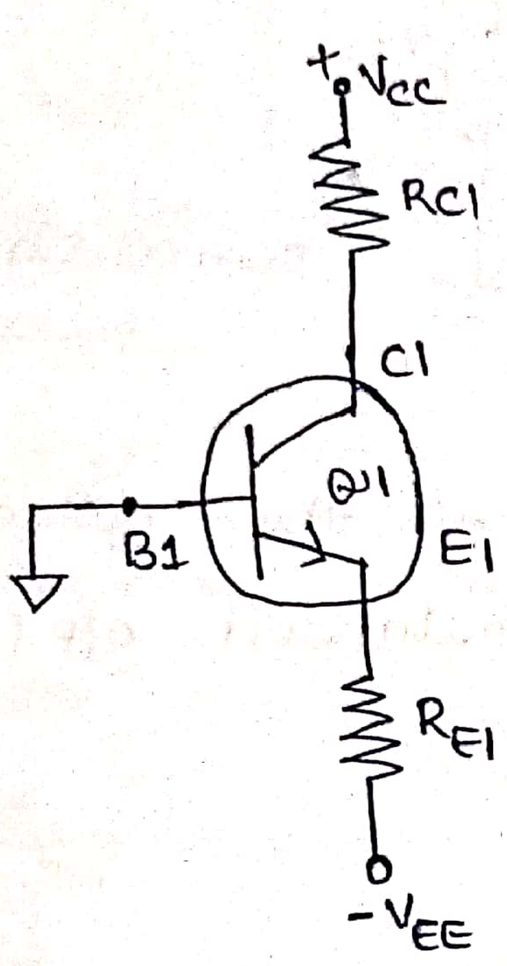

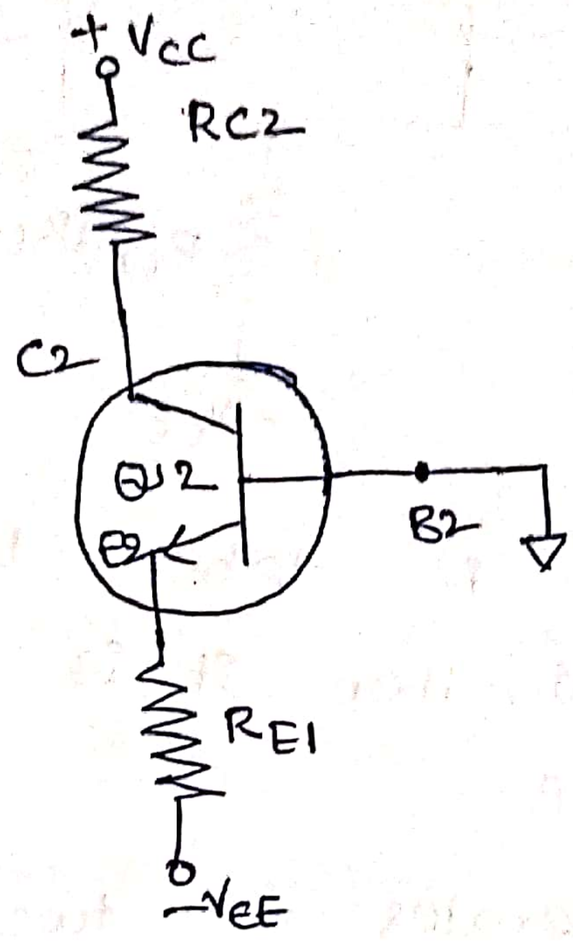

→ The two transistors Q1 & Q2 are having exactly matched characteristics.

→ the two collector and emitter resistances R_{C1}, R_{C2}, R_{E1} and R_{E2} are equal.

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∴ the magnitudes must be equal

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→ If the collector o/p is taken between two collector terminals without any ground, then it is called as balanced o/p (or) double ended o/p (or) floating o/p.

* with the help of center tapped transformer, we are getting two signals with same magnitude and has 180° phase shift.
* Assume that, the sine wave on the base of Q1 is positive going while on the base Q2 is negative going. with a positive going on the base of Q1, an amplified negative going signal develops on the collector of Q1.
* Due to positive going signal, current through R_E increases and hence a positive going wave is developed across R_E because of emitter follower action of Q1.
* Due to negative going signal on the base of Q2, an amplified positive going signal, develops on the collector of Q2 and hence a negative going signal develops across R_E because of emitter follower action of Q2.
* The signal voltages across R_E, due to the effect of Q1 and Q2 are equal in magnitude & 180° out of phase.
* Hence, these two signals cancel each other & there is no signal across the emitter resistance. Hence, there is no a.c flows through the R_E.

i.e; $I_E = 0$

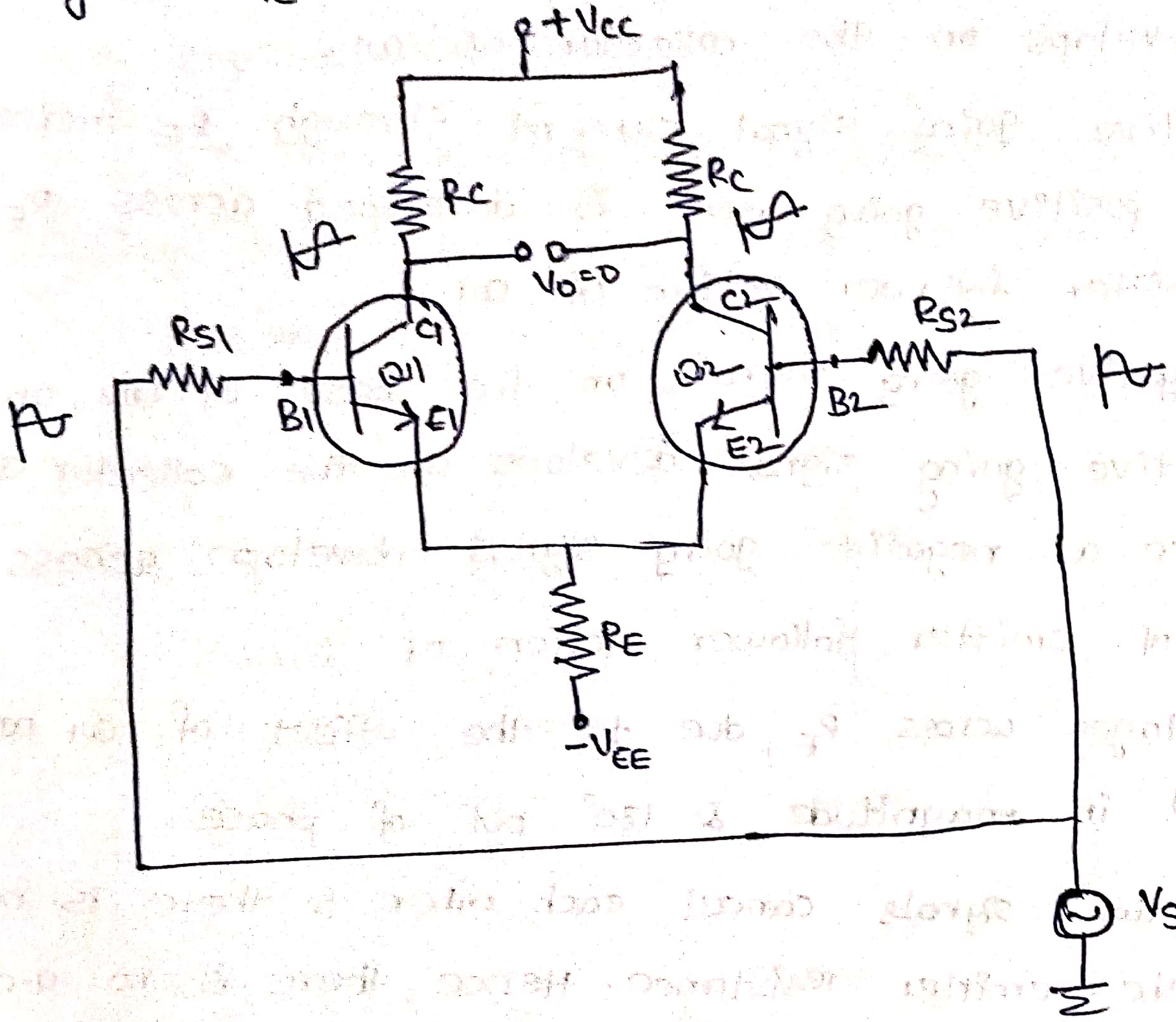
* V_o is the o/p taken across collector of Q1 and Q2. the two o/p's on collector 1 & 2 are equal in magnitude but opposite polarity. V_o is the difference b/w these two signals.

Ex:- 10 - (-10) = 20

* Hence, the difference voltage o/p V_o is twice the voltage of single ended o/p.
* In this mode, R_E does not introduce negative feedback.

Common mode operation :-

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. The two i/p signals are equal in magnitude and phase. The circuit diagram is.



* the base B_1 of transistor Q1 and base B_2 of transistor Q2 is a positive going signal. since the circuits are emitter biased, the same signal voltages appear across R_E, which adds together.

* Hence, R_E carries a signal current and provides negative feedback. This feedback reduces the common mode gain of DA.

* The two o/p signals across Q1 and Q2 are having same magnitude and are in phase each other.

Ex:- 10 - 10 = 0.

∴ the difference o/p voltage, V_o is almost zero & neglibily small. But ideally it is zero.

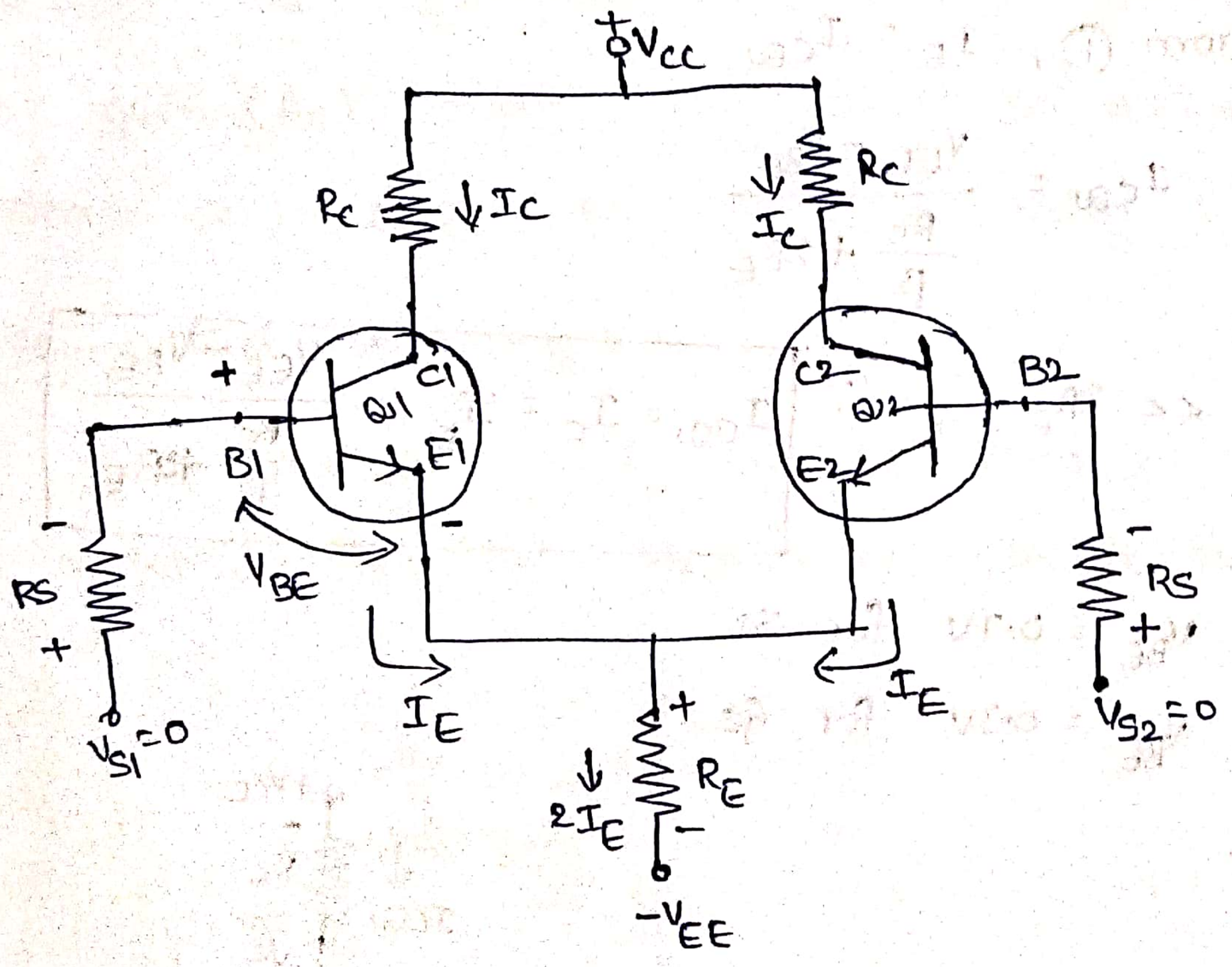
DC Analysis of Differential amplifier :-

* DC analysis means to obtain the operating point values i.e; I_{CQ} & V_{CEQ} for the transistors used.

* the V_{CC} and V_{EE} are d.c supply voltages while the input signals are A.C.

* the DC equivalent circuit can be obtained by reducing the i/p a.c signals to zero.

* the DC equivalent circuit is



∴ the circuit is symmetrical and the two transistors are matched, so it is enough to find out operating point I_{CQ} and V_{CEQ} for any one of the transistor i.e; consider only half circuit.

To find I_{CQ} :-

Apply KVL to Base emitter loop of Q1,

$$-V_{S1} + I_B R_S + V_{BE} + 2I_E R_E - V_{EE} = 0 \quad \rightarrow (i)$$

W.K.T. $V_{S1} = 0$, $I_C = \beta I_B$

$$\therefore \quad \boxed{I_{CQ} \cong I_C \cong I_E} \quad \rightarrow (1)$$

$$I_E = \beta I_B \implies I_B = \frac{I_E}{\beta} \rightarrow (2)$$

substitute eq-(1) & (2) & $V_{S1} = 0$ in eq-(1)

$$\frac{I_E}{\beta} R_S + V_{BE} + 2 I_E R_E - V_{EE} = 0$$

$$I_E \left[\frac{R_S}{\beta} + 2R_E\right] = V_{EE} - V_{BE}$$

From (1), $I_E = I_{CQ}$

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}$$

$\because \frac{R_S}{\beta} << 2R_E$, $\therefore$ $\boxed{I_{CQ} = I_C = I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}}$

$V_{BE} = 0.7V$ for Si

$V_{BE} = 0.3V$ for Ge

To find V_{CEQ} :-

W.K.T. $V_{CE} = V_C - V_E \rightarrow (3)$

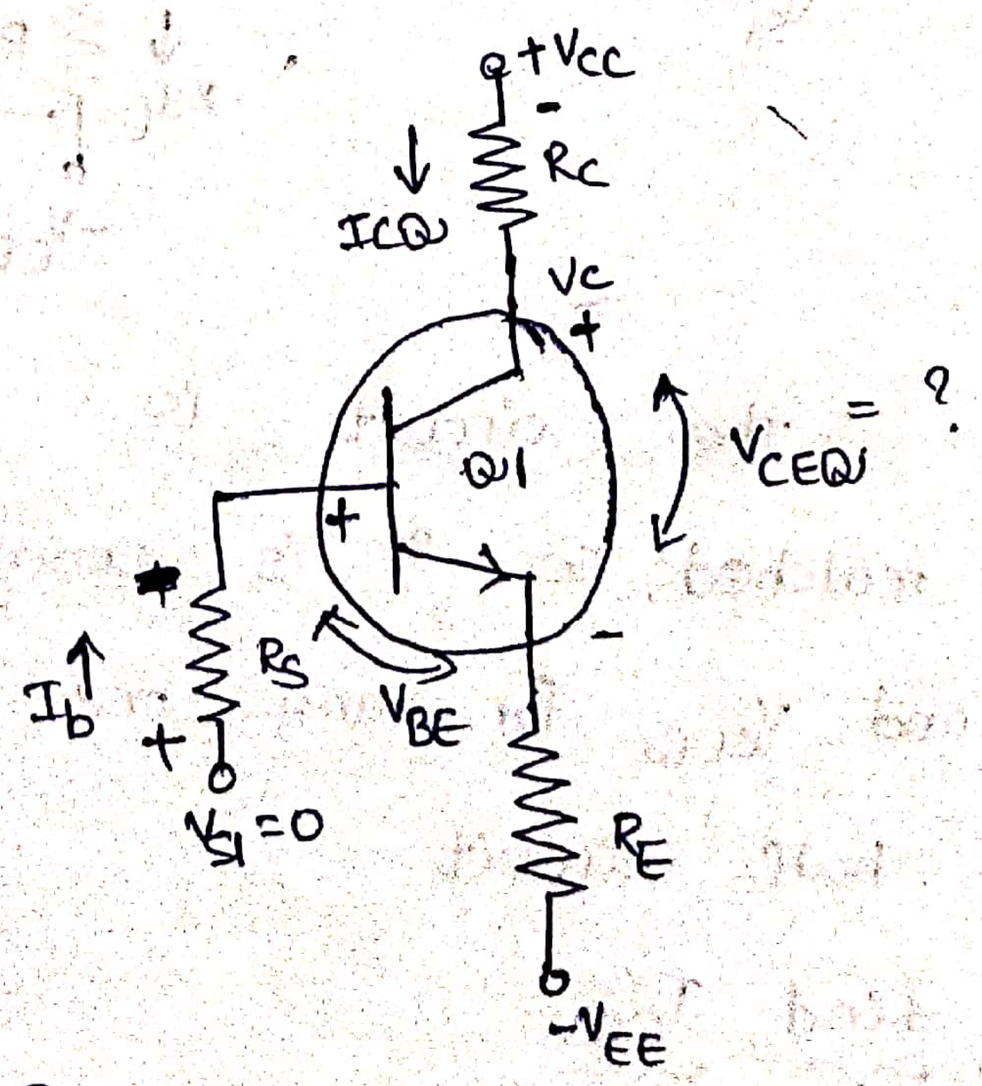
At the output, KVL

$$-V_{CC} + I_{CQ} R_C + V_C = 0$$

$$V_C = V_{CC} - I_{CQ} R_C \rightarrow (4)$$

Sub. V_C in eq-(3)

$$V_{CE} = V_{CC} - I_{CQ} R_C - V_E \rightarrow (5)$$



At input,

$$I_b R_S + V_{BE} + V_E = 0$$

Ignore $I_b R_S$, $V_E = -V_{BE} \rightarrow (6)$

substitute eq-⑥ in eq-⑤

$$V_{CEQ} = V_{CE} = V_{CC} - I_{CQ}R_C + V_{BE} \rightarrow (7)$$

→ DC Analysis is same for remaining differential Amplifiers.

AC analysis of differential amplifier :-

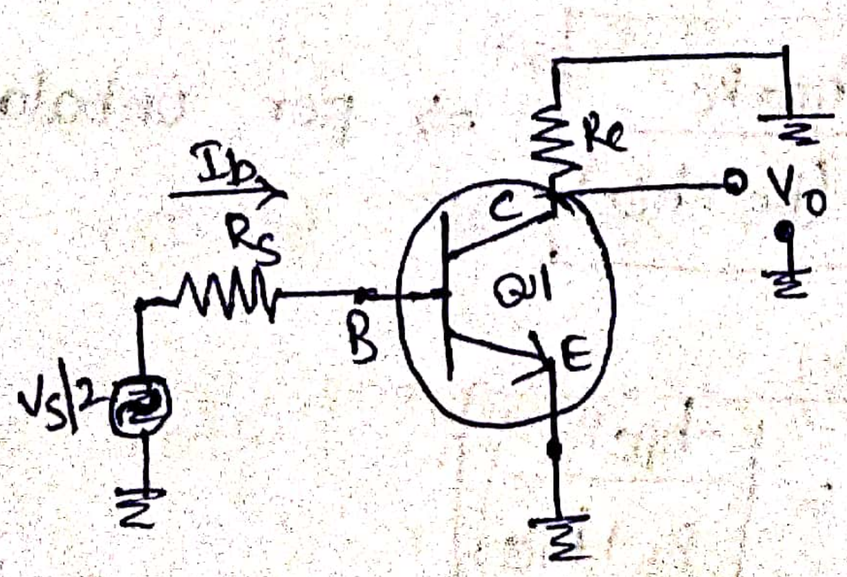
* AC analysis means consider a.c signal and make d.c signals zero.

* Two transistors are matched, so consider half circuit.

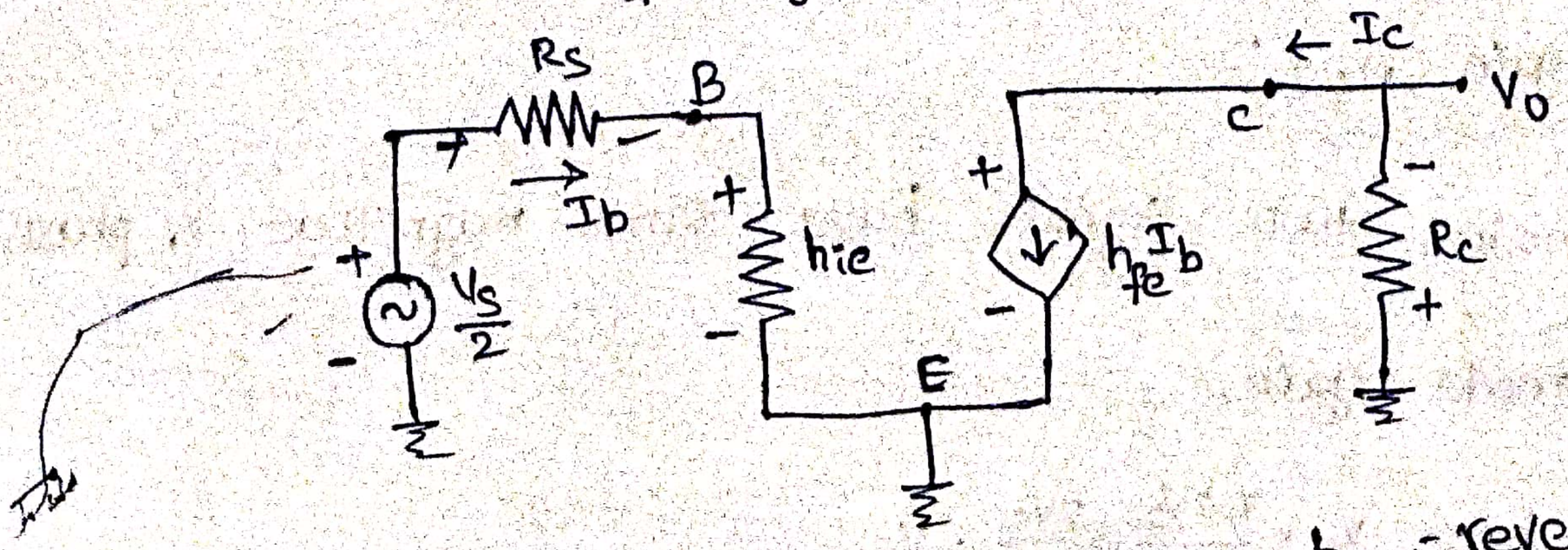
* Here we calculate differential gain (A_d), common mode gain (A_c), input impedance (or) resistance (R_i), output resistance (R_o), CMRR of the DA using h-parameters.

① Differential gain (A_d) :-

consider half circuit because two transistors are matched. The a.c equivalent circuit for one transistor is



the appropriate hybrid model for above fig. is shown below, by neglecting h_{re} & h_{oe}.



Here, h_{ie} = i/p impedance, h_{re} = reverse voltage gain

h_{fe} = forward current, h_{oe} = o/p admittance.

W.K.T. $A_d = \left|\frac{V_o}{V_d}\right|$

V_d is the difference voltage,

$$V_d = V_1 - V_2 = \frac{V_S}{2} - \left(\frac{-V_S}{2}\right) = V_S$$

$$A_d = \left|\frac{V_o}{V_S}\right|$$

output voltage, $v_o = -I_c R_c$

From circuit, I_c is $h_{fe} I_b$

$$\therefore V_o = -h_{fe} I_b R_c \rightarrow (1)$$

Apply KVL to i/p loop,

$$\frac{-V_S}{2} + I_b R_S + I_b h_{ie} = 0$$

$$V_S = 2 I_b (R_S + h_{ie}) \rightarrow (2)$$

$\frac{\text{eq}(1)}{\text{eq}(2)}$, $\frac{V_o}{V_S} = \frac{-h_{fe} I_b R_c}{2 I_b (R_S + h_{ie})}$

$$\boxed{A_d = \left|\frac{V_o}{V_S}\right| = \frac{-h_{fe} R_c}{2(R_S + h_{ie})}} \Rightarrow \text{For unbalanced o/p}$$

For balanced o/p,

$$\boxed{A_d = \left|\frac{V_o}{V_S}\right| = \left|\frac{-h_{fe} R_c}{R_S + h_{ie}}\right|}$$

$$A_d\big|_{\text{balanced o/p}} = 2\, A_d\big|_{\text{unbalanced o/p}}.$$

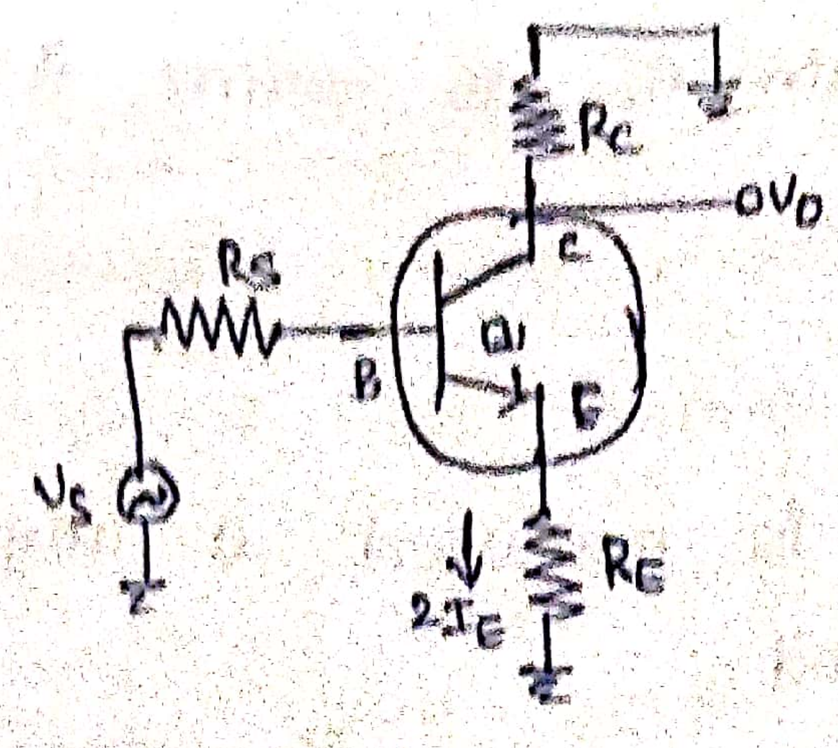
② common mode gain (A_c) :-

* In this mode, two signals have same magnitude & phase.

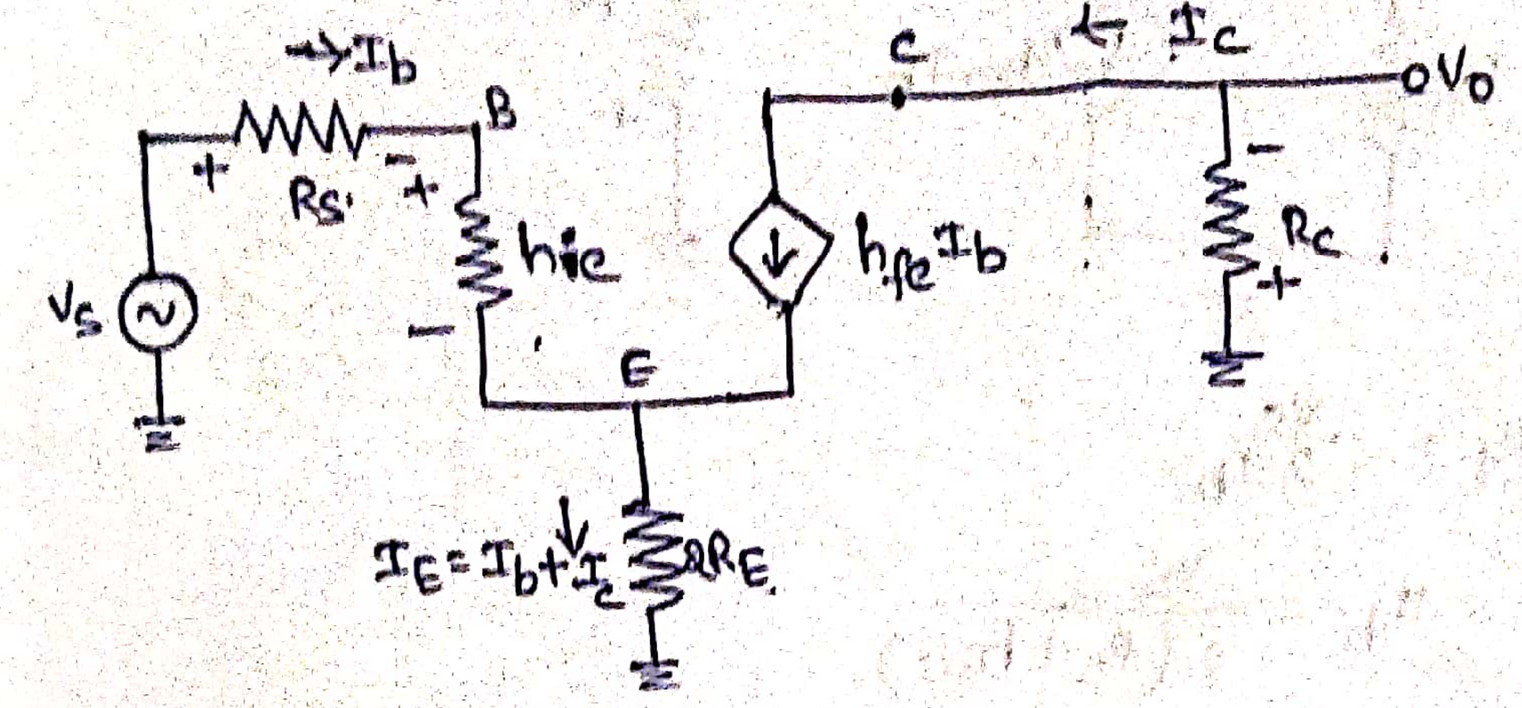
the common mode gain,

$$A_c = \frac{V_o}{V_c} \quad \text{but} \quad V_c = \frac{V_1 + V_2}{2} = \frac{2V_S}{2} = V_S$$

$$\therefore A_c = \left|\frac{V_o}{V_S}\right|$$



The approximate model for above circuit, ignoring hoe, hre is



The o/p voltage is given by, $V_o = -I_c R_c$

from circuit, $I_c = h_{fe} I_b$

$$\therefore V_o = -h_{fe} I_b R_c \rightarrow (1)$$

Apply KVL at i/p loop,

$$-V_s + I_b R_s + I_b h_{ie} + 2R_E (I_b + I_c) = 0$$

$$-V_s + I_b R_s + I_b h_{ie} + 2R_E (I_b + h_{fe} I_b) = 0$$

$$-V_s + I_b \left(R_s + h_{ie} + 2R_E (1 + h_{fe}) \right) = 0$$

$$V_s = I_b \left(R_s + h_{ie} + 2R_E + 2R_E h_{fe} \right) \rightarrow (2)$$

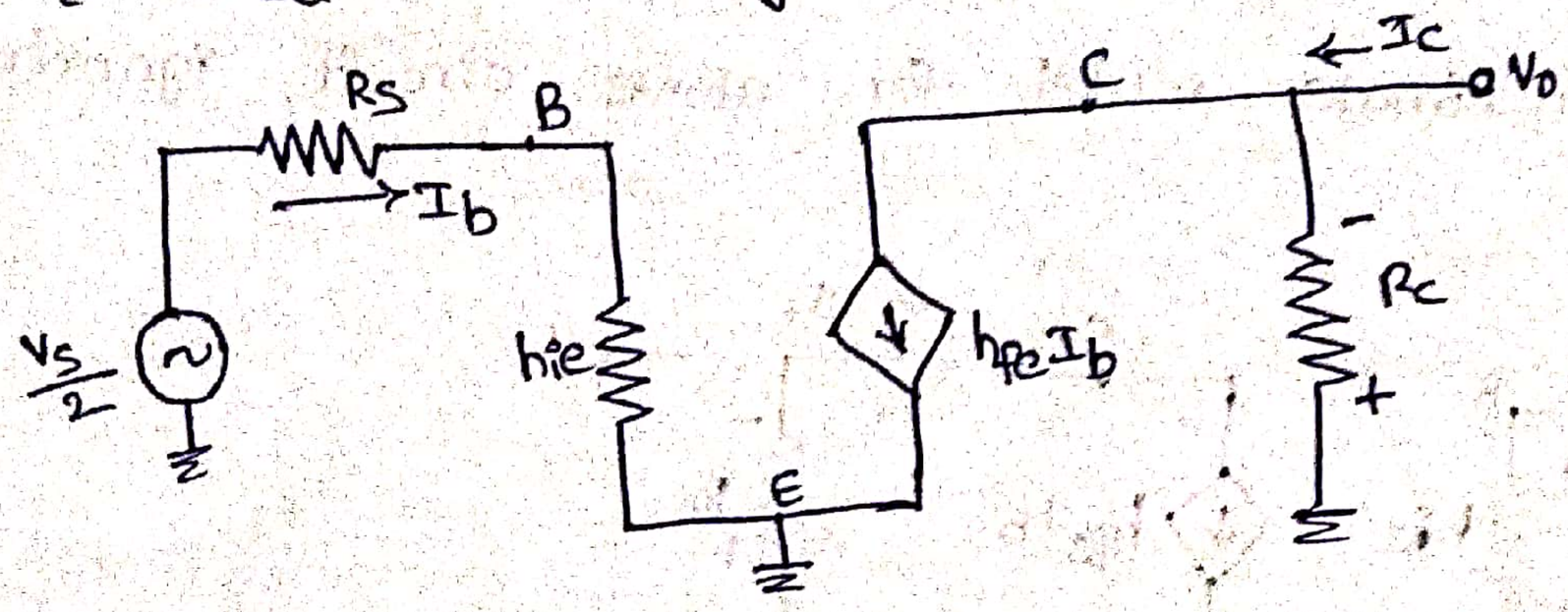
$$\frac{\text{eq-}(1)}{\text{eq-}(2)} \rightarrow \frac{V_o}{V_s} = \frac{-h_{fe} I_b R_c}{I_b \left(R_s + h_{ie} + 2R_E (1 + h_{fe}) \right)}$$

$$\therefore A_c = \left| \frac{V_o}{V_s} \right| = \frac{-h_{fe} R_c}{R_s + h_{ie} + 2R_E (1 + h_{fe})}$$

* the common mode gain A_c is same for both balanced & unbalanced o/p.

⑤ i/p impedance :-

the i/p impedance is measured at any one of the i/p terminal w.r.t. ground.



$$R_i = \frac{V_s}{2I_b}$$

W.K.T, $$I_b = \frac{V_s}{2(R_s + h_{ie})}$$

$$R_i = \frac{V_s}{2 \cdot \frac{V_s}{2(R_s + h_{ie})}}$$

$$\boxed{R_i = R_s + h_{ie}}$$

For single input, $R_I = R_s + h_{ie}$

For dual input, $R_I = 2(R_s + h_{ie})$

output impedance :-

the o/p impedance of the circuit is measured at o/p w.r.t ground.

∴ output impedance, $R_o = R_c$.

CMMR :-

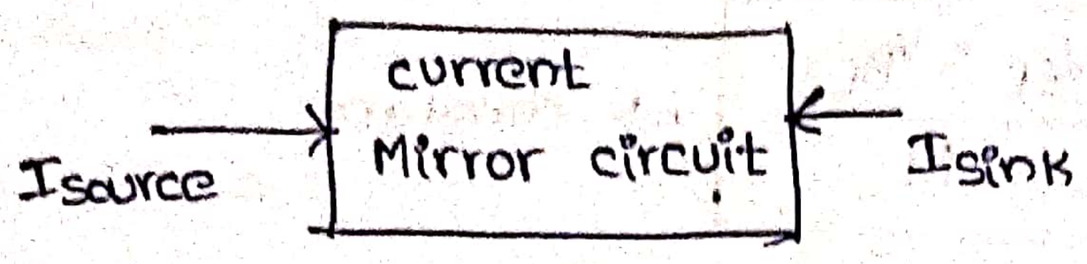
W.K.T. $$CMRR = \frac{A_d}{A_c}$$

and $$A_d = \frac{R_c h_{ie}}{R_s + h_{ie}}, \quad A_c = \frac{R_c h_{fe}}{R_s + h_{ie} + 2R_E(1 + h_{fe})}$$ for dual i/p balanced o/p DA

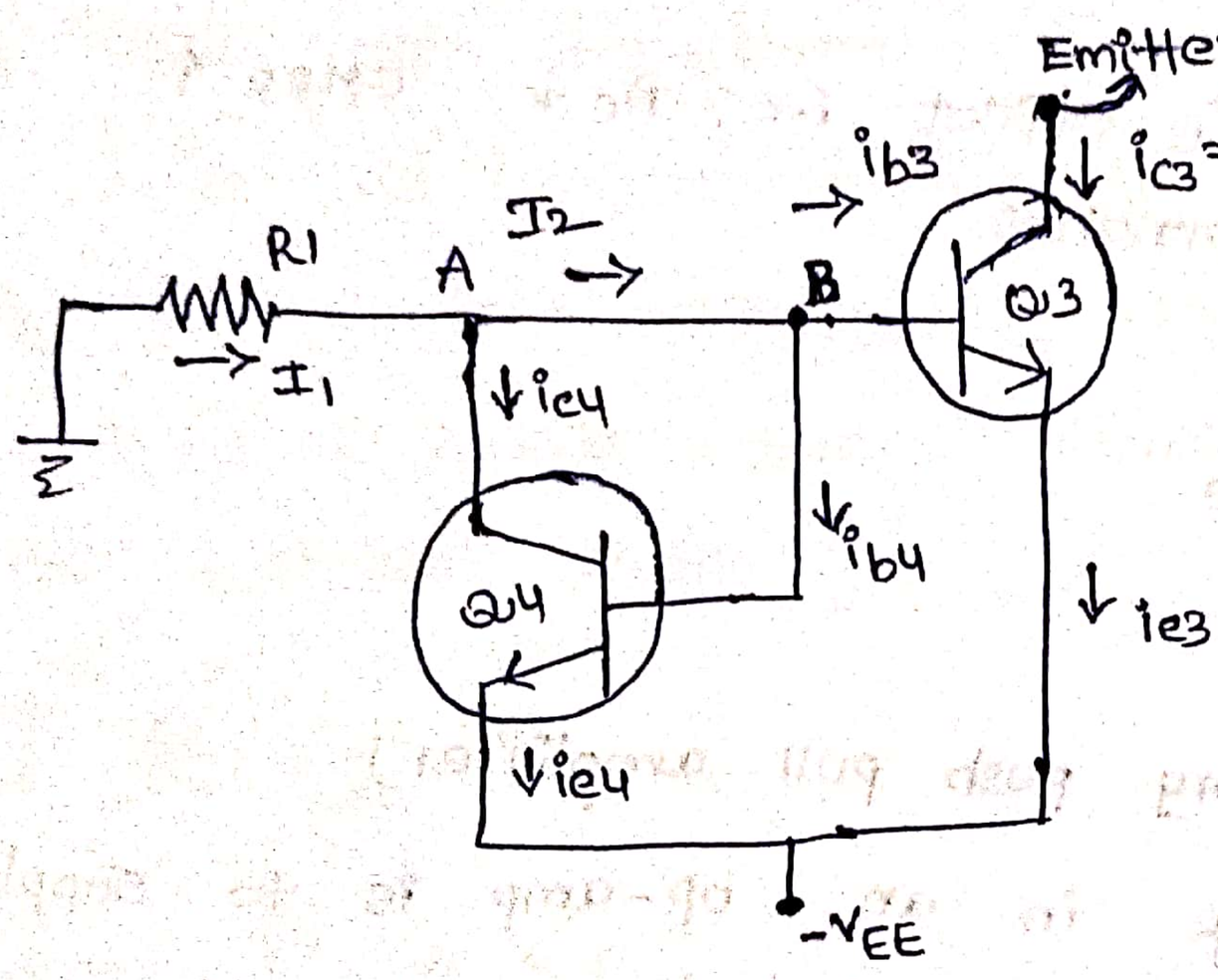
so $$CMRR = \frac{R_s h_{ie} + 2R_E(1 + h_{fe})}{R_s h_{fe}}$$

current mirror circuit :-

current mirror circuit means, o/p current is mirror image of i/p current.



$I_{source} = I_{sink}$ = constant.



Q3, Q4 are matched transistors.,

$i_{e3} = i_{e4}$; $i_{C3} = i_{C4}$; $i_{b3} = i_{b4}$; $V_{BE3} = V_{BE4}$

KCL at node A,

$$I_1 = I_2 + i_{C4} \longrightarrow (1)$$

KCL at node B,

$$I_2 = i_{b3} + i_{b4}$$

$$I_2 = 2i_{b3} \longrightarrow (2) \quad [\because i_{b3} = i_{b4}]$$

∵ From (1),

$$I_1 = 2i_{b3} + i_{C4} = 2i_{b3} + i_{C3}$$

$$I_1 = \frac{2i_{C3}}{\beta} + i_{C3} \qquad \left[\because i_b = \frac{i_C}{\beta}\right]$$

$$I_1 = i_{C3}\left[\frac{2}{\beta} + 1\right]$$

Since β is very high, $\frac{I}{\beta}$ is ignored.

$$I_1 = i_{C3} = \text{constant}$$

KVL of Q3 transistor

$$I_1 R_1 + V_{BE3} - V_{EE} = 0$$

$$\boxed{I_1 = \frac{V_{EE} - V_{BE3}}{R1}} \Rightarrow \text{constant}$$

Advantages:-

* Provides increasing R_E effect i.e; Ac ↓ CMRR ↑
* Less number of components.
* Easy to design
* Easy to manufacture
* Temperature stability.

output stage :- (complementory push pull amplifier)

* The o/p stage in an op-amp is to supply the load current & provide a low impedance o/p. ideally the total supply voltage is $V_{CC} + V_{EE}$.

* output stage consists of two complimentory transistors Q1 (npn) and Q2 (pnp) connected as shown in fig.

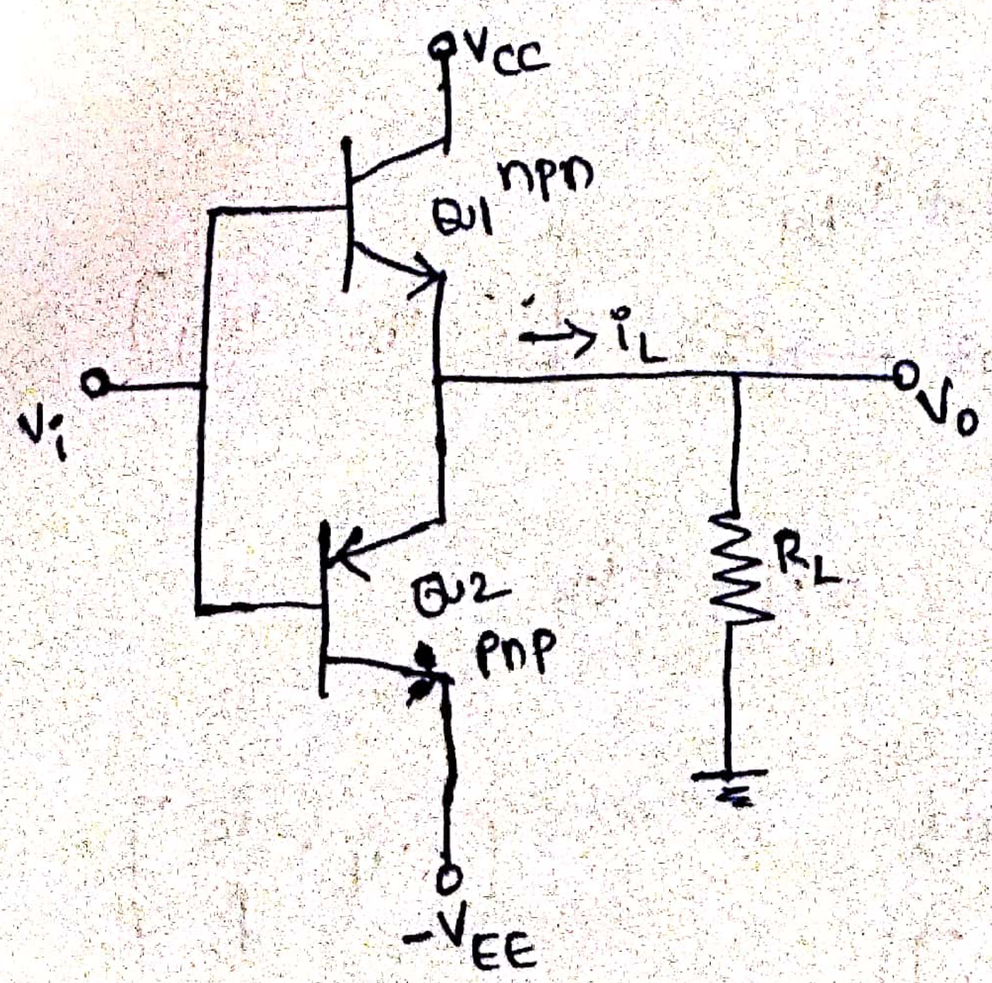


fig:- complementary stage of DA.

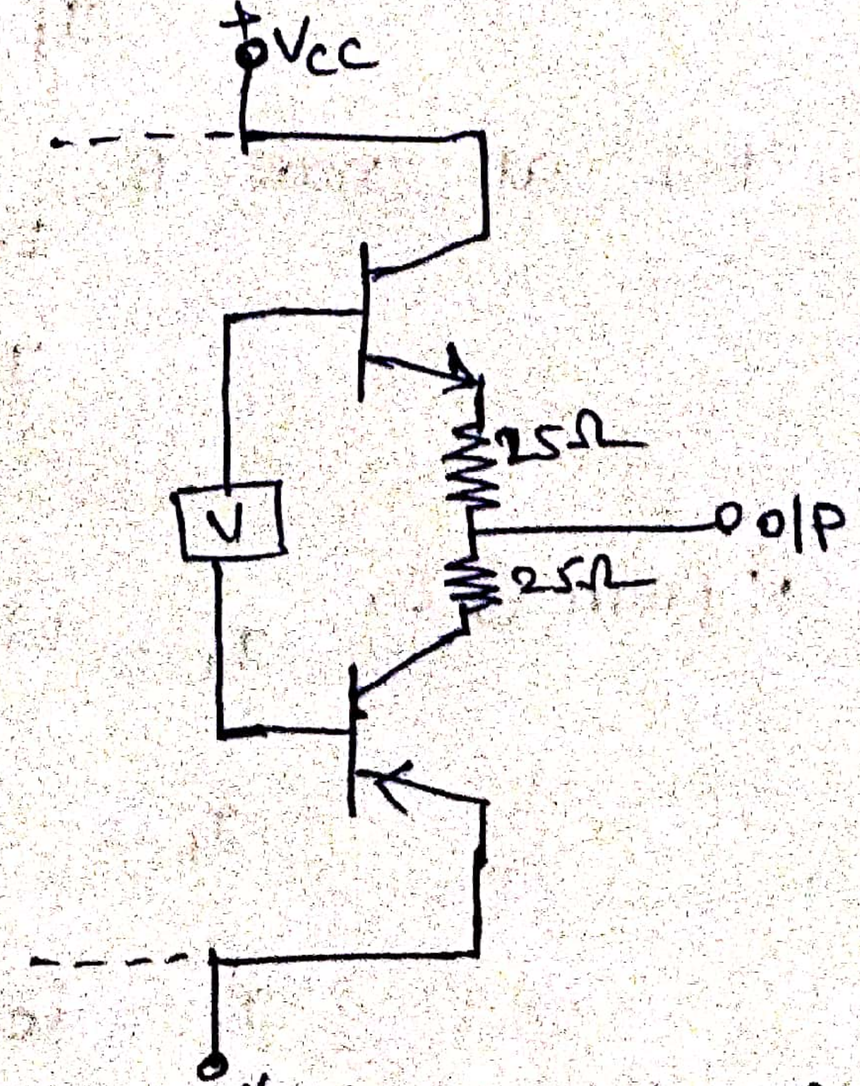


fig:- o/p stage of IC741

* For V_i positive, Q1 is ON and supplies current to load R_L.

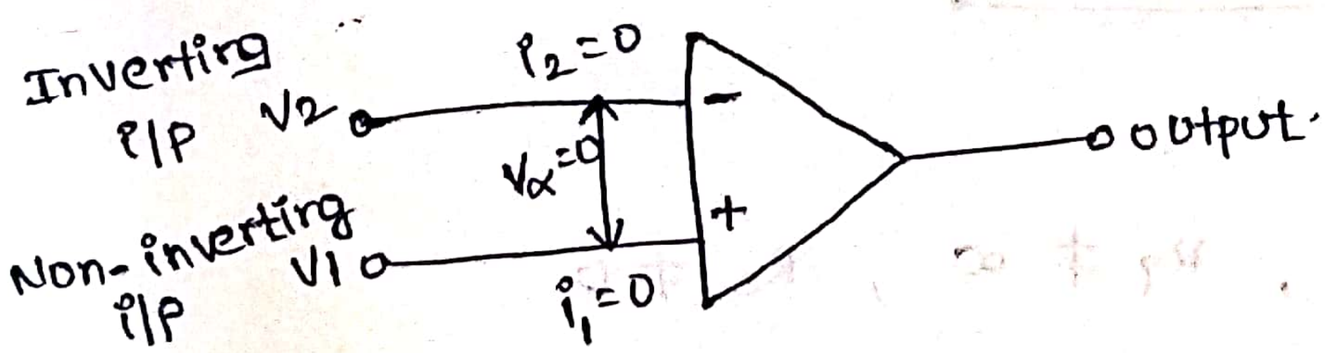
* For V_i negative, Q1 is cut-off & Q2 acts as a sink to remove current from load R_L.

* The limitation in this is, the o/p V_o remains zero until the i/p V_i exceeds V_{BE} (cut in) = 0.5V. This is called "cross over distortion".

* It can be eliminated by applying a bias voltage V slightly greater than $2V_{BE(cut-in)} = 1V$ b/w two bases.

* so, a small current flows in the transistors even in the quiescent state.

Ideal OP-Amp :-



* If $V_1 = 0$, then V_o is 180° out of phase with the i/p signal V_2.

* If $V_2 = 0$, then V_o will be inphase with the i/p signal applied at V_1.

* the ideal op-amp characteristics are

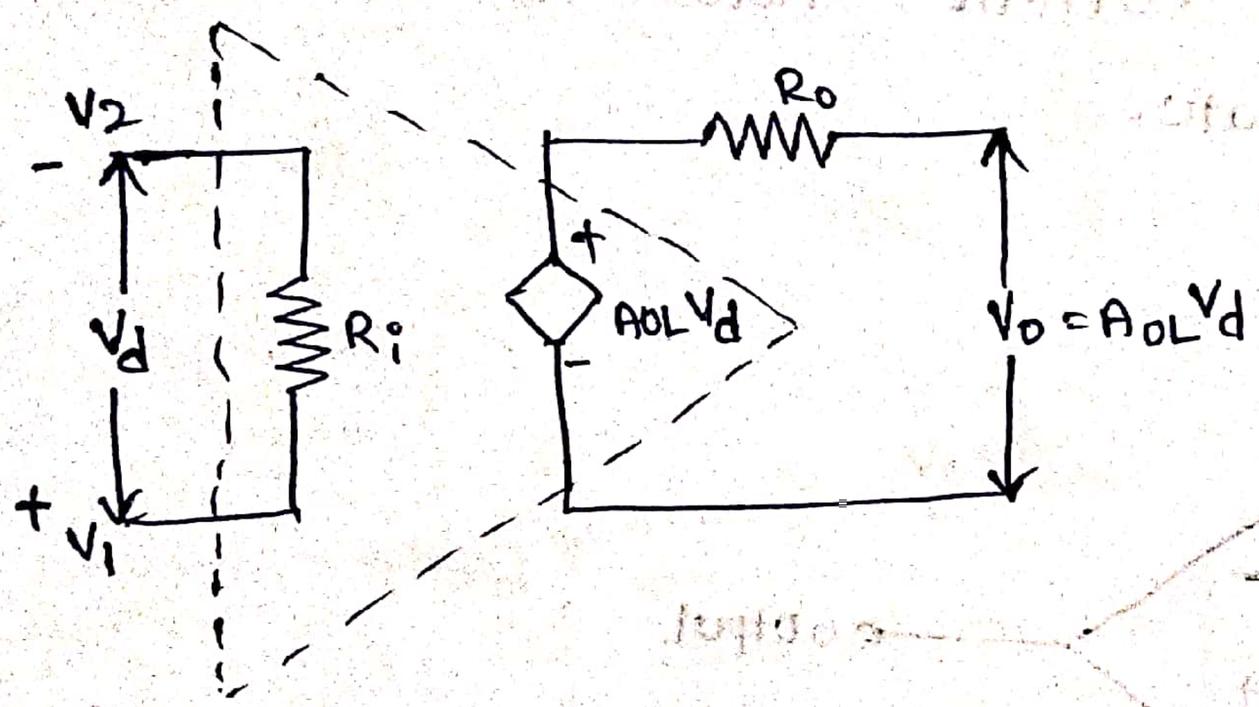
1. open loop voltage gain (A_{OL}) = ∞
2. Input resistance, $R_i = \infty$
3. o/p resistance, $R_o = 0$
4. Bandwidth = ∞
5. offset voltage = 0

* Because of ∞ input impedance, the ideal op-amp draws no current at both the i/p terminals. i.e; $I_1 = I_2 = 0$.

* since gain is infinity, the differential i/p voltage between inverting & non-inverting terminal, $V_d = V_1 - V_2$ is zero for finite o/p voltage.

* the o/p voltage V_o is independent of the o/p current as $R_o = 0$. Thus "o/p" can drive infinite no. of other devices.

* the physical op-amp is not an ideal one, the equivalent circuit is.



where, $A_{OL} \neq \infty$, $R_i \neq \infty$, $R_o \neq 0$.

Here, the o/p is a voltage controlled voltage source, $A_{OL} V_d$ is the equivalent thevinen voltage source.

R_o is the equivalent thevinen resistance.

$\therefore$ o/p voltage, $V_o = A_{OL} \cdot V_d$

$$V_o = A_{OL}(V_1 - V_2)$$

where, V_o = o/p voltage

A_{OL} = open loop gain

V_d = differential voltage.

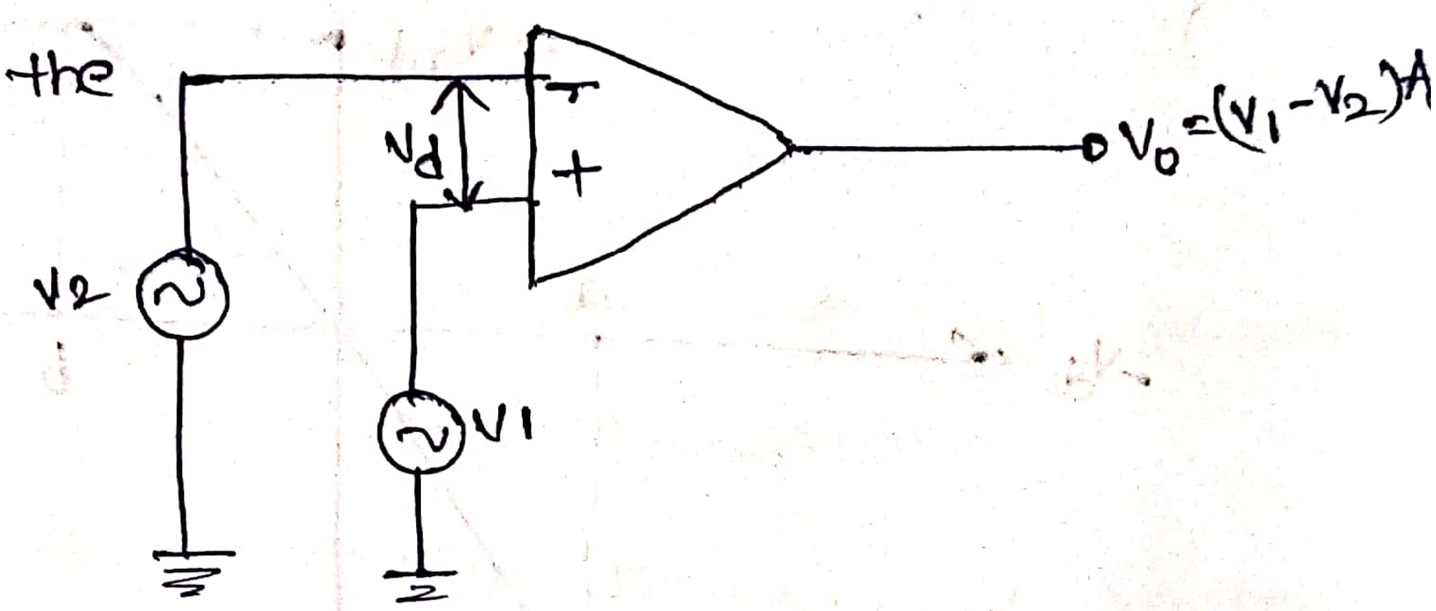
Voltage Transfer Characteristics of Ideal op-amp :-

Ideally op-amp open loop gain is infinite. Thus for zero i/p, the o/p of op-amp is always at saturation level, i.e; $\pm V_{sat}$.

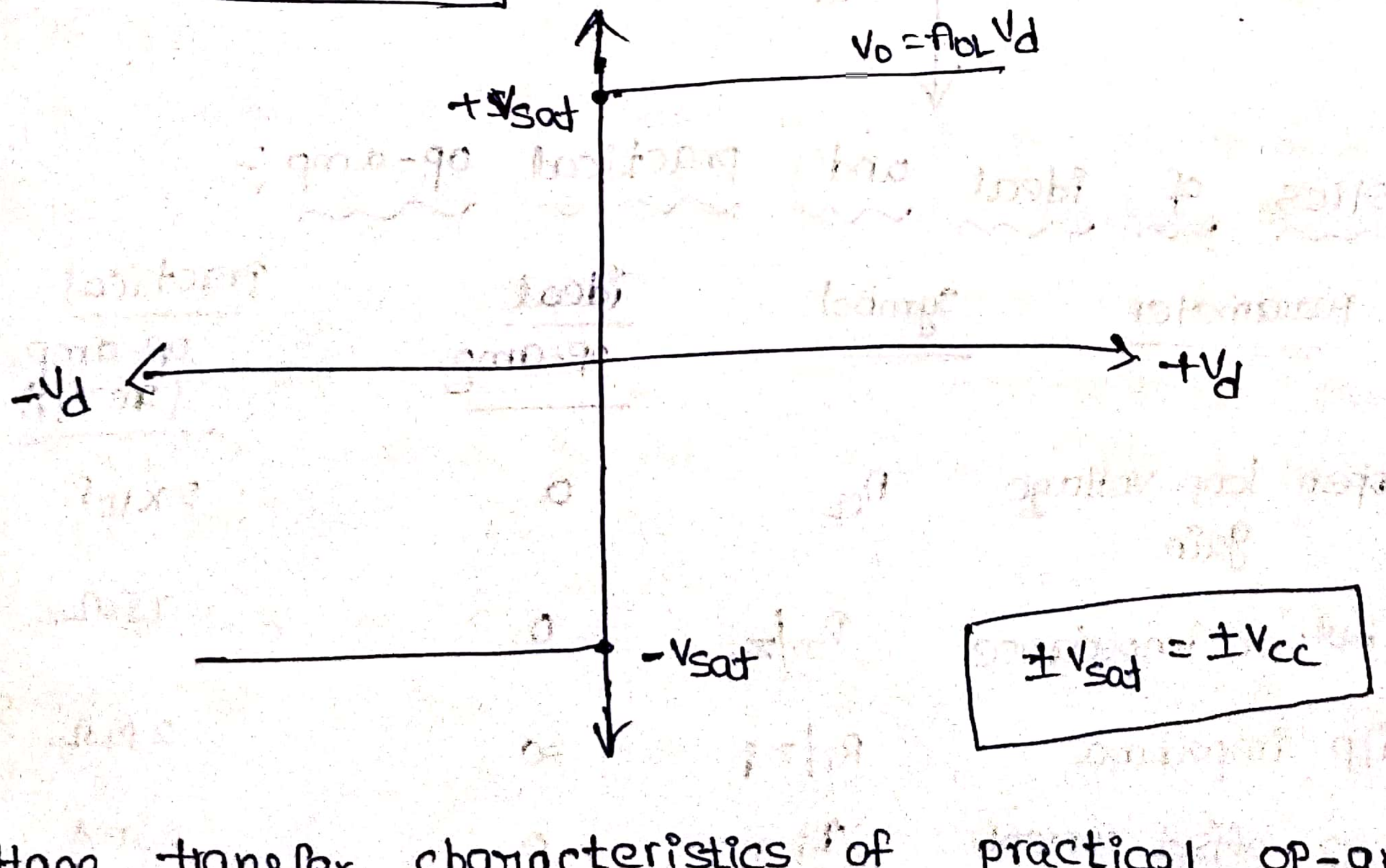
If $V_1 > V_2$ then $V_o = +V_{sat}$

If $V_1 < V_2$ then $V_o = -V_{sat}$.

* the o/p assume one of the two possible states. i.e; $+V_{sat}$ (or) $-V_{sat}$ and o/p acts as a switch.



$\therefore A_{OL} = \infty$



$\pm V_{sat} = \pm V_{cc}$

voltage transfer characteristics of practical op-amp :-

* The utility of an op-amp can be greatly increases by providing a -ve feedback.

* The o/p in this stage is not drives into saturation and circuit becomes linear manner

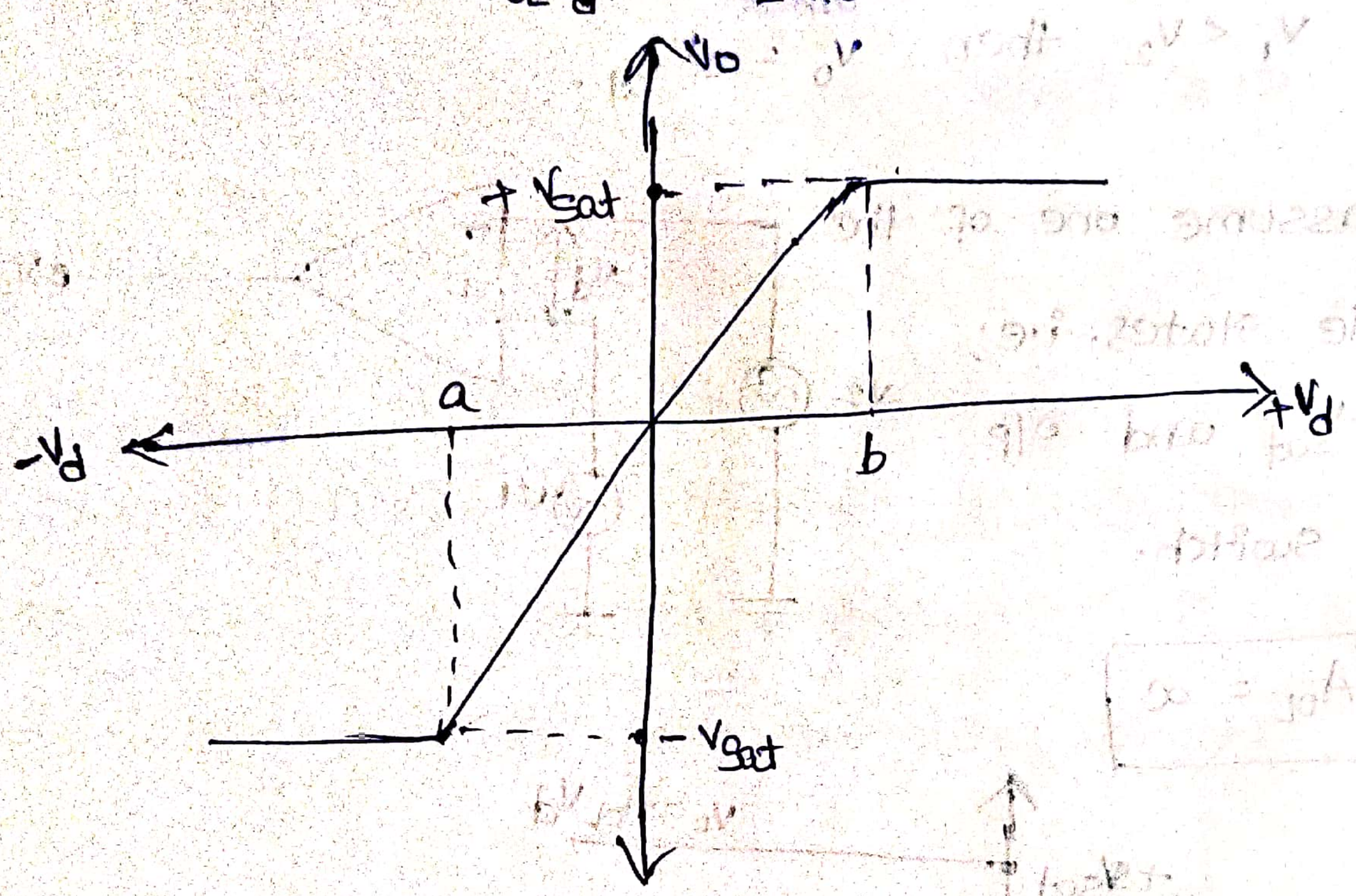
*practically the A_{OL} is finite. for op-amp 741C it is 2×10^5

$$V_o = A_{OL} V_d$$

$$+V_{sat} = 2\times10^5 V_d$$

Saturation voltages are ±15V

$$V_d = \frac{V_o}{A_{OL}} = \frac{\pm15V}{2\times10^5} = \pm75\mu V$$



characteristics of ideal and practical op-amp :-

S.NO.	parameter	symbol	ideal op-amp	practical op-amp. (IC741)
1.	open loop voltage gain	A_{OL}	∞	2×10^5
2.	output impedance	R_o/z_o	0	75Ω
3.	i/p impedance	R_i/z_i	∞	2MΩ
4.	i/p offset current	I_{ios}	0	20nA
5.	i/p offset voltage	V_{ios}	0	1MV
6.	Bandwidth	B.W	∞	1MHZ
7.	CMRR	ρ	∞	90dB.
8.	slew rate	S	∞	0.5V/μs

9	i/p bias current	I_B	0	80nA
10	Power supply rejection ratio	PSRR	0	30μV/V

D.C characteristics of op-Amp :-

DC characteristics means to find

① Input bias current (I_B) ② Input offset voltage (V_{ios})

③ Input offset current (I_{ios}) ④ Thermal drift

① Input bias current (I_B) :-

* the ideal op-amp i/p terminals does not drawn any current because of infinite i/p impedance.

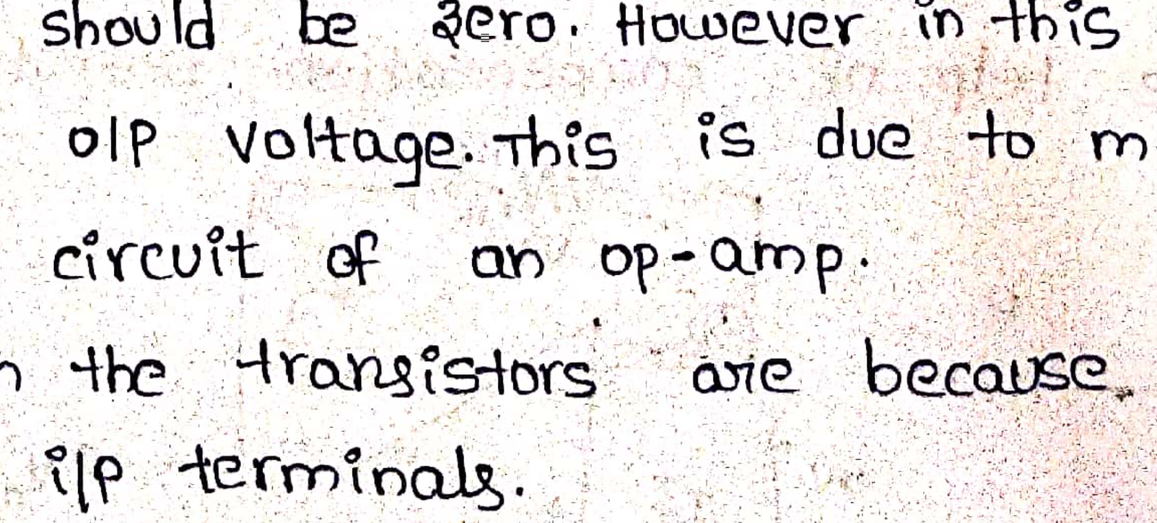
* The i/p stage of the op-amp is the dual i/p DA and the i/p terminals are the base terminals of the two transistors.

* whenever both the i/p terminals of an op-amp are grounded, Ideally the o/p voltage should be zero. However in this condition op-amp shows a small o/p voltage. this is due to mismatching present in the internal circuit of an op-amp.

* the mismatching in the transistors are because of the current present in the i/p terminals.

* The average value of the two currents flowing into the op-amp i/p terminals called "input bias current" and denotes as "I_B"

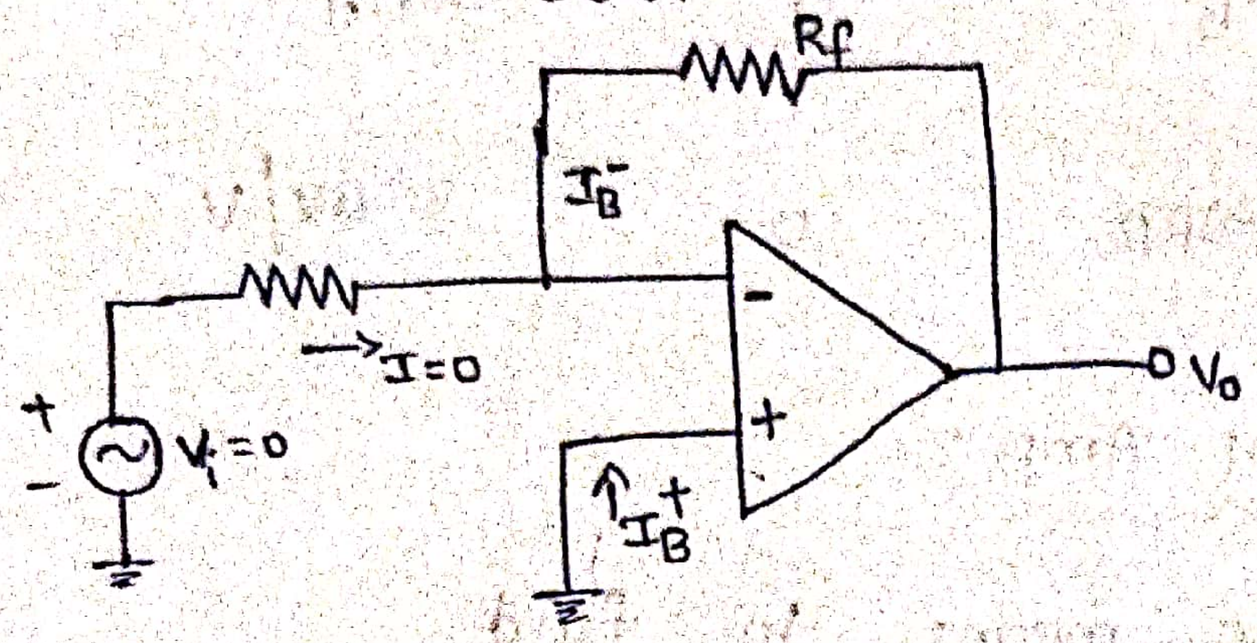
$$I_B = \frac{I_{b1} + I_{b2}}{2}$$



where,

I_B is temperature dependent.

Effect of i/p bias current :-



The o/p voltage is given by $V_o = I_B^- R_f$

→ for IC741 op-amp the i/p bias current is 80nA

For BJT the value of resistance is 1MΩ

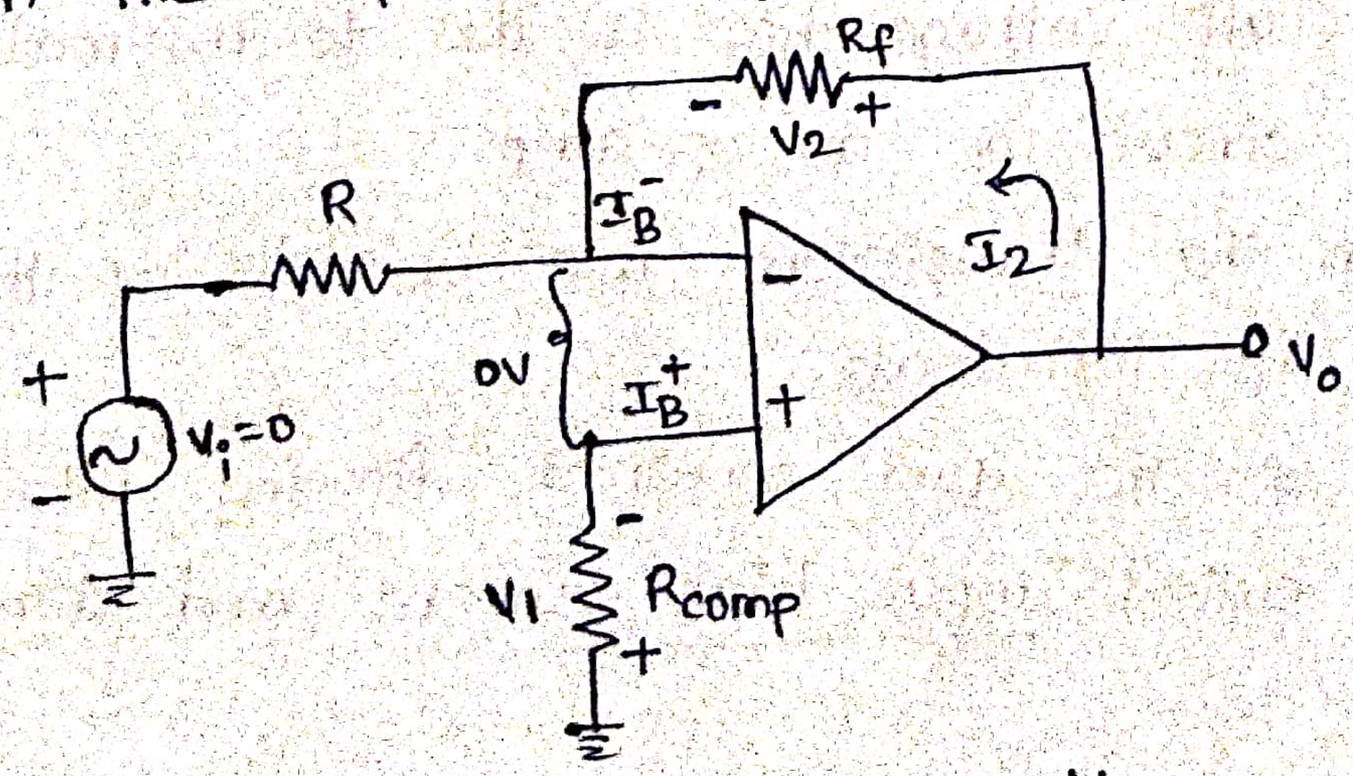
$$V_o = I_B^- R_f$$

$$= 80nA \times 1M\Omega$$

$$V_o = 80mV$$

→ For zero i/p signal, the o/p also must be zero but due to the i/p bias current the o/p voltage is 80mV.

→ whenever, we are measuring the o/p signal in mv. This becomes the serious issue. Now the problem can be rectified with the help of compensation resistor R_{comp}.



Apply KVL, $-V_1 + 0 + V_2 - V_o = 0$

$$\boxed{V_o = V_2 - V_1}$$

→ For proper value of R_f the value of V_2 is get cancelled with V_1 and makes the o/p as zero.

Derivation of R_{comp} resistor :-

In generally, we are assuming that $\boxed{I_B^+ = I_B^-}$ → (1)

$$\frac{V_1}{R_{comp}} = I_B^+ \longrightarrow (2)$$

$$I_B^- = I_1 + I_2 \rightarrow (3)$$

$$I_1 = \frac{V_1}{R_1} \rightarrow (4)$$

$$I_2 = \frac{V_2}{R_f} \rightarrow (5)$$

W.K.T. $V_0 = V_2 - V_1 \longrightarrow (6)$

Now, for $V_1 = 0$ then $V_0 = 0$

$$V_2 - V_1 = 0$$

$$\boxed{V_2 = V_1} \rightarrow (7)$$

(7) in (5)

$$I_2 = \frac{V_1}{R_f} \rightarrow (8)$$

(8), (4), (3).

$$I_B^- = \frac{V_1}{R_1} + \frac{V_1}{R_f} = V_1\left[\frac{R_f + R_1}{R_1 R_f}\right] \longrightarrow (9)$$

(9), (2) in (1)

$$I_B^+ = I_B^- \Rightarrow \frac{V_1}{R_{comp}} = V_1\left[\frac{R_1 + R_f}{R_1 R_f}\right]$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} \longrightarrow (10)$$

$$= R_1 \,||\, R_f .$$

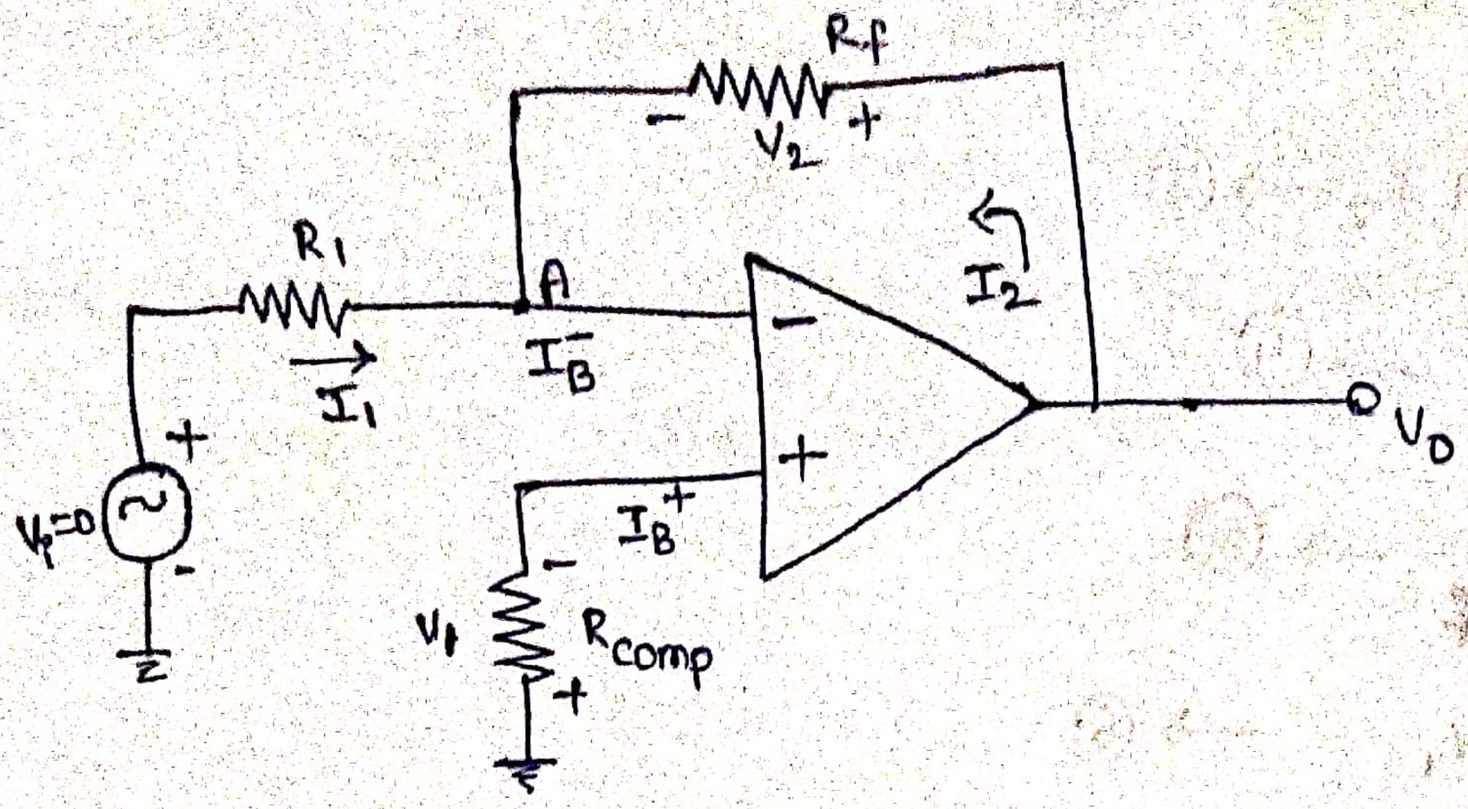
Input offset current (I_{ios}) :-

Bias current compensation will work only when $I_B^+ = I_B^-$. But practically those 2 are not equal and the amount of difference b/w I_B^+ and I_B^- is called "Input offset current"

The i/p offset current is

$$I_{ios} = \left| I_B^+ - I_B^- \right|$$

Now let us examine the effect of i/p offset current.



The o/p voltage of the above ckt is,

$$V_o = I_2 R_f - V_1 \rightarrow (1)$$

$$V_1 = I_B^+ R_{comp} \rightarrow (2)$$

Apply KCL at node 'A'

$$I_2 = I_B^- - I_1 \rightarrow (3)$$

$$I_1 = \frac{V_1}{R_1} \rightarrow (4)$$

Sub. (2) in (4)

$$I_1 = \frac{I_B^+ R_{comp}}{R_1} \rightarrow (5)$$

(5) in (3)

$$I_2 = I_B^- - \frac{I_B^+ R_{comp}}{R_1} \rightarrow (6)$$

(3), (2) in (1)

$$V_o = \left[I_B^- - \frac{I_B^+ R_{comp}}{R_1} \right] R_f - I_B^+ R_{comp} \rightarrow (7)$$

To design a T network we first pick up

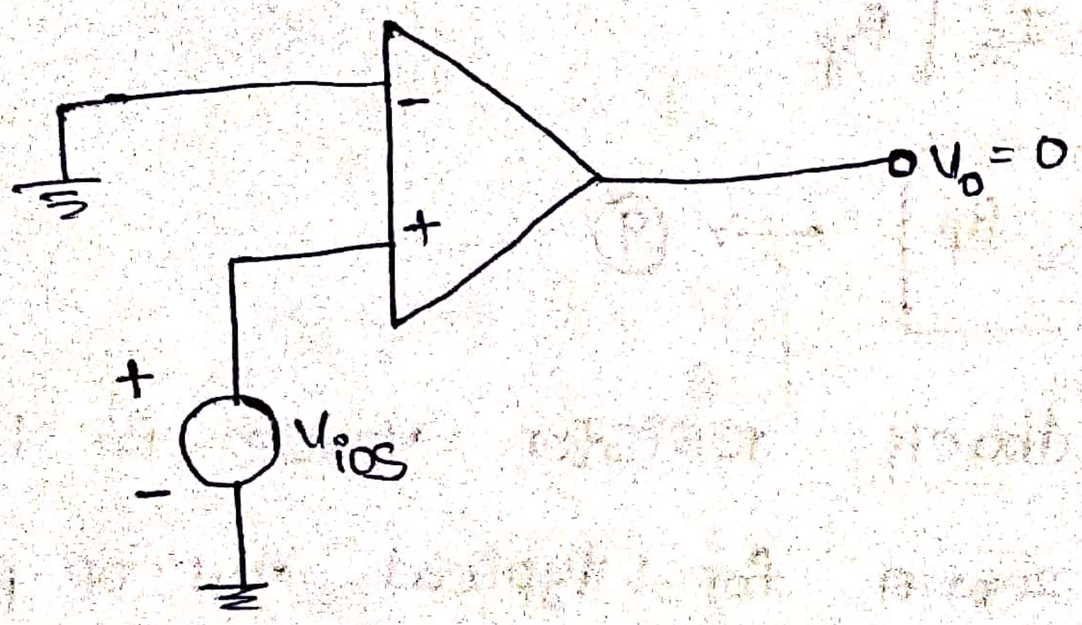
$$R_t << \frac{R_f}{2}$$

$$R_s = \frac{R_t^2}{R_f \cdot 2R_t}$$

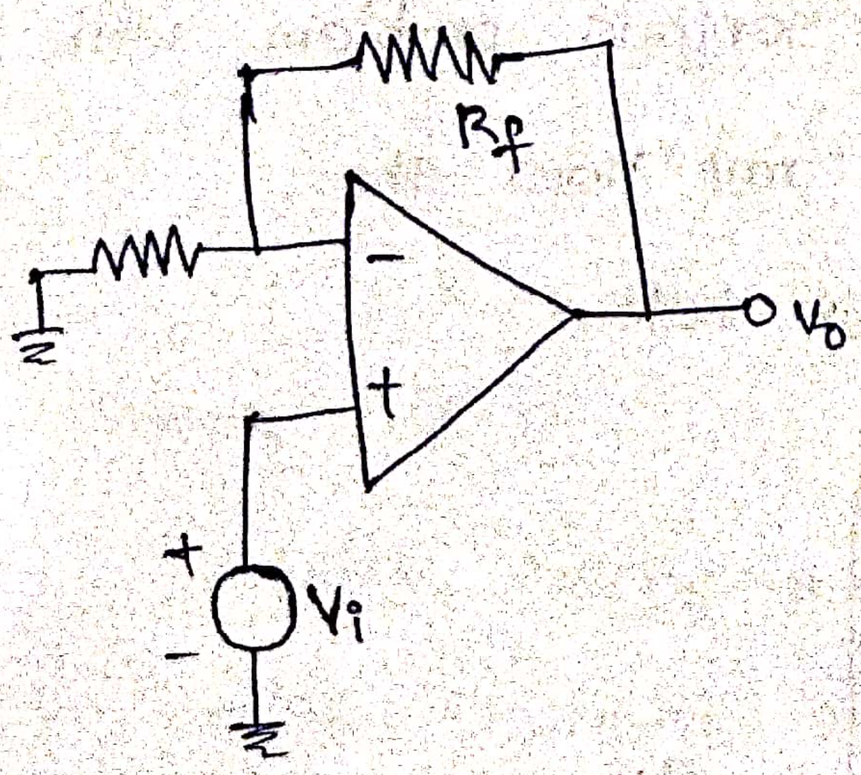
Input offset Voltage (V_{ios}) :-

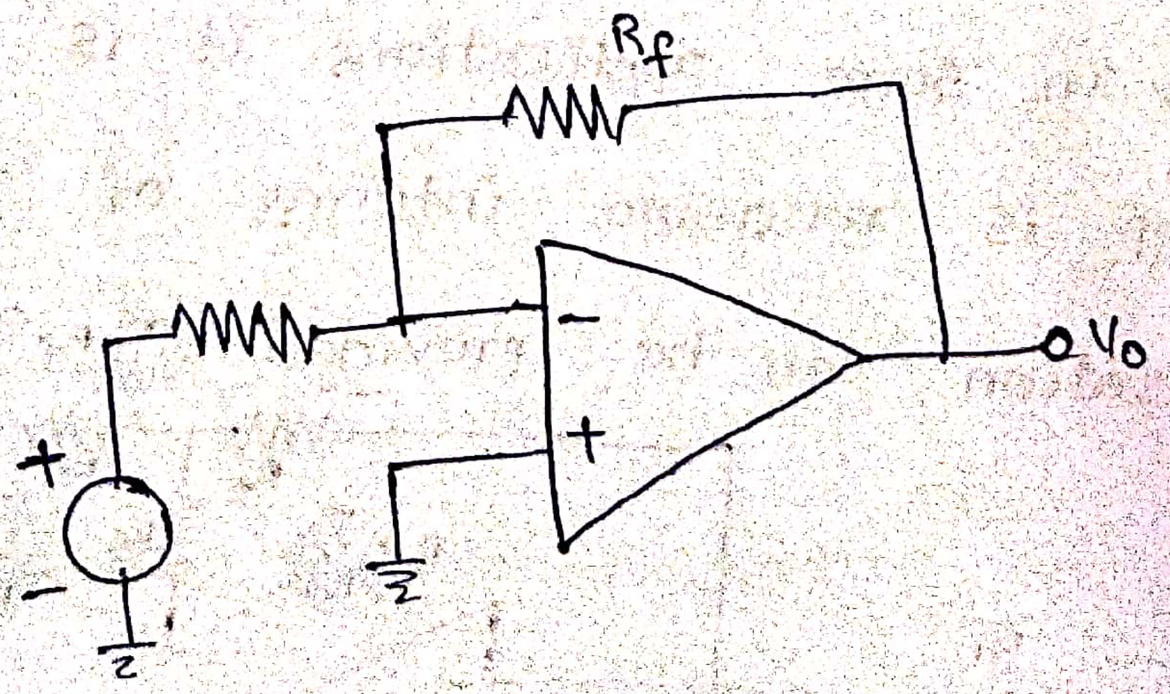
* Even though we are providing the compensation there exist a small amount of the o/p voltage due to unavailable in balance in the op-Amp.

* To bring the o/p voltage as zero we are applying a small amount of i/p voltage at either terminals of op-Amp is called (V_{ios}) and it is shown as below.

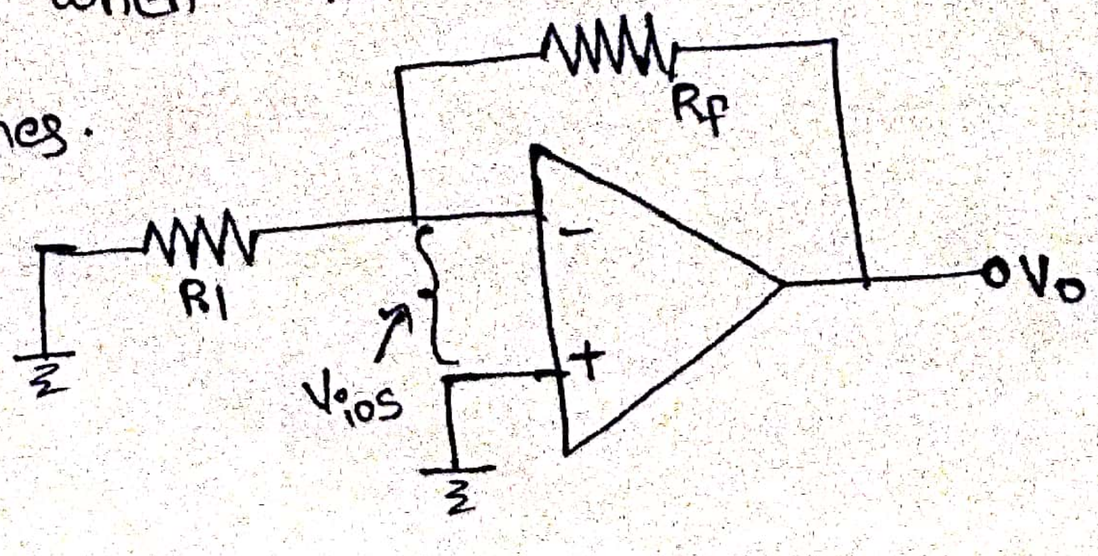


Let us examine the effect of i/p offset voltage on inverting and non-inverting op-Amp as follows.





when the i/p signal is zero, then both the ckt becomes.



when $V_i = 0$

W.K.T. $R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$ ⟶ (8)

Sub. (8) in (7)

$$V_o = I_B^- - \frac{\left[\frac{R_1 R_f}{R_1 + R_f}\right]}{R_1} I_B^+ - I_B^+ \left(\frac{R_1 R_f}{R_1 + R_f}\right)$$

$$R_1 V_o = I_B^- R_1 - \left(\frac{R_1 R_f}{R_1 + R_f}\right) I_B^+ - R_1 I_B^+ \left(\frac{R_1 R_f}{R_1 + R_f}\right)$$

$$= \left[I_B^- - I_B^+ \right| R_f$$

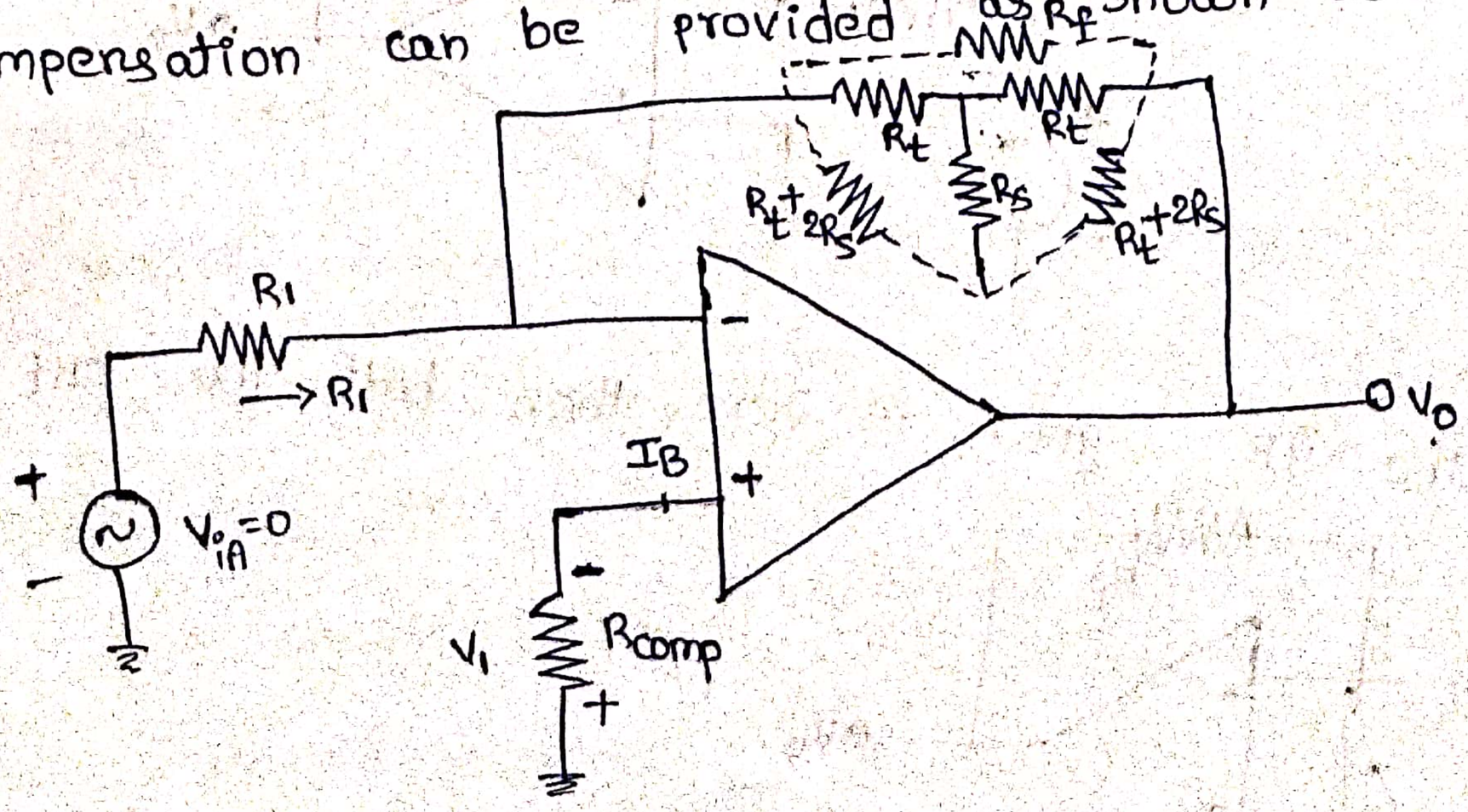
$$V_o = \left| I_B^- - I_B^+ \right| R_f$$

$$\boxed{V_o = I_{ios} \cdot R_f} \longrightarrow (9)$$

→ If the feedback resistor value is 1MΩ and i/p offset current is 200nA for typical 741 op-Amp using BJT then the o/p voltage is

$$\boxed{V_o = 200\,mV}$$

→ In some applications it is a serious problem with the o/p is measure interms of the mv how the compensation can be provided as shown below.



→ The i/p resistance of op-Amp is high for that the value of R_1 is also high, Too high gain and R_f value is also large.

→ Now the designing of the ckt for the compensation is as follows.

$$R_f = \frac{R_t^2 + 2R_t R_s}{R_s}$$

From the circuit, the voltage $V_2 = V_o \frac{R_1}{R_1 + R_f} \rightarrow (1)$

$$\frac{V_2 (R_1 + R_f)}{R_1} = V_o$$

$$V_o = V_2 \left(1 + \frac{R_f}{R_1}\right)$$

From circuit, $V_{ios} = |V_i - V_2|$

$= |0 - V_2|$

$= |-V_2|$

$V_{ios} = V_2 \longrightarrow (3)$

$$\boxed{V_o = V_{ios} \left(1 + \frac{R_f}{R_1}\right)} \longrightarrow (4)$$

Thermal Drift :-

* Drift means a function of temperature.

* Bias current, offset current and offset voltage changes with temperature.

* A circuit carefully nulled at 25°c may not remain when the temperature rises to 35°c. This is called drift.

* An offset current drift is expressed in nA/°C.
* An offset voltage drift is expressed in mV/°C.
* This indicate the charge in offset for each degree celsius charge in temperature.
* There are very few circuit techniques that can be used to minimize the effect of drift.
* Forced air cooling may be used to stabilise the ambient temperature.

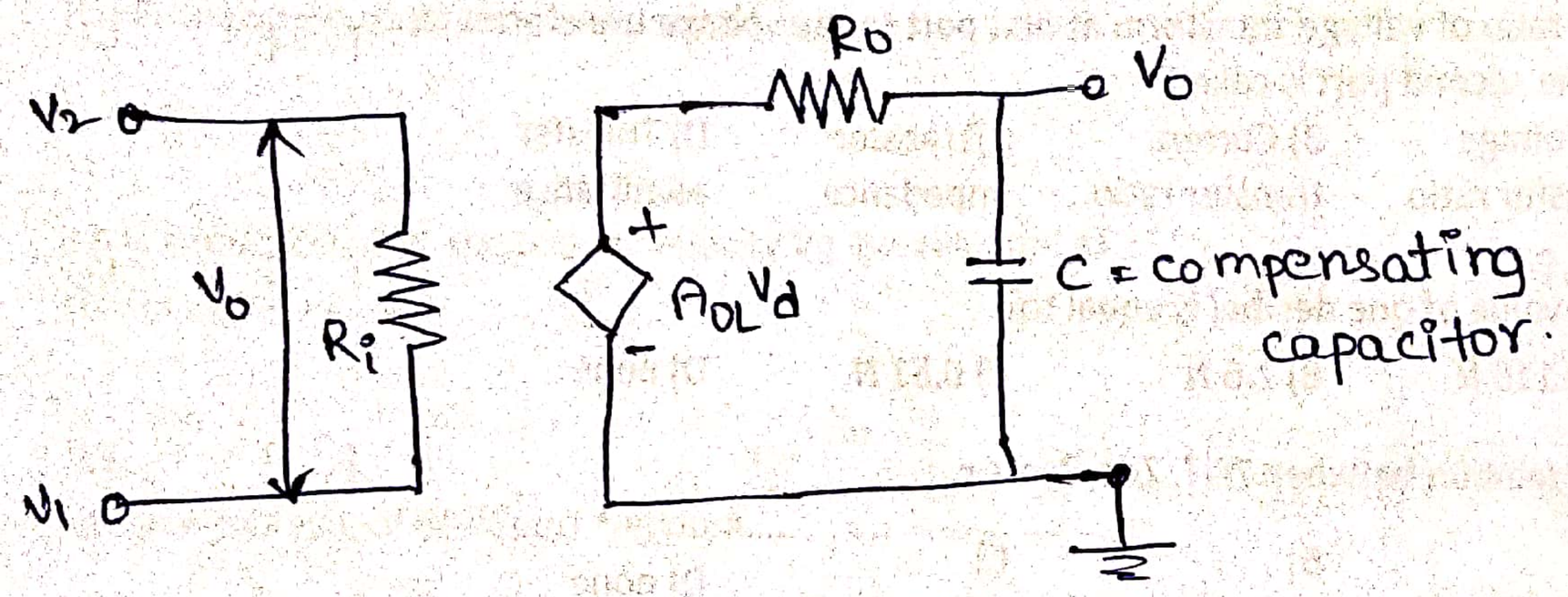
A.C characteristics of op-Amp :-

The important A.C characteristics of op-Amp are

1. Frequency response 2. Slew Rate.

1. Frequency response :-

For ideal op-amp the bandwidth is ∞ that means the gain is constant upto infinity but for practical op-amp the gain decreases as the freq. increases.



Let $-jx_c$ be the capacitive reactance due to capacitor. From the above fig. to get V_o, apply voltage division rule "V_o"

$$V_o = A_{OL}V_d\left(\frac{-jx_c}{R_o - jx_c}\right)$$

W.K.T, $\quad -j = \frac{1}{j}$, $X_c = \frac{1}{2\pi fC}$

$$\therefore V_o = A_{OL}V_d\left(\frac{\frac{1}{j2\pi fC}}{R_o + \frac{1}{j2\pi fC}}\right)$$

$$= A_{OL}V_d\left[\frac{\frac{1}{j2\pi fC}}{\frac{R_o j2\pi fC + 1}{j2\pi fC}}\right]$$

$$V_o = A_{OL}V_d\left[\frac{1}{1 + j2\pi R_o fC}\right]$$

Let $f_1 = \frac{1}{2\pi R_0 C}$

$$A_{OL}(f) = \frac{V_o}{V_d} = \frac{A_{OL}}{1+j(f/f_1)}$$

the magnitude of A is

$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}}$$

the phase angle ϕ of A is

$$\phi = -\tan^{-1}[(f/f_1)]$$

→ from the magnitude it can be seen that

(i) for the freq $f \ll f_1$

the magnitude of gain is $20 \log A_{OL}$ in dB

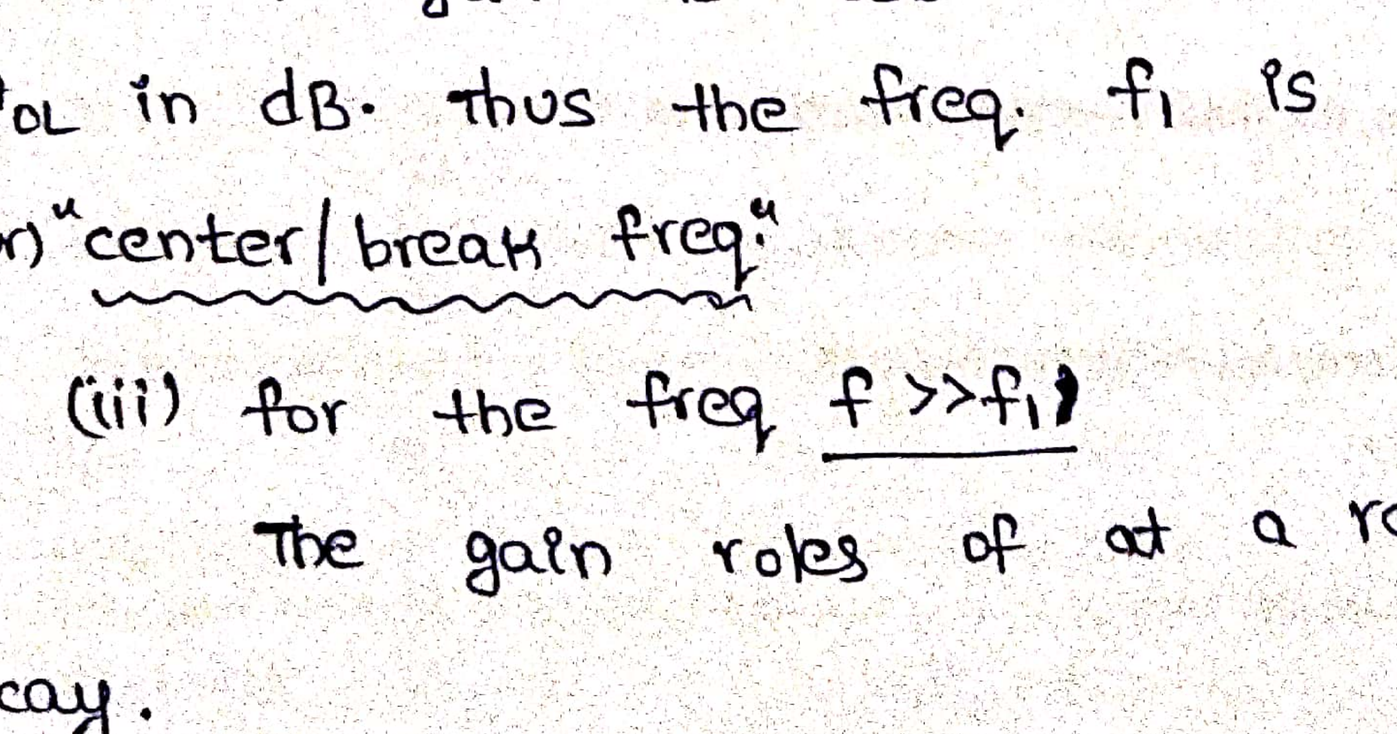
(ii) At the freq $f = f_1$

the gain is 3dB down from the dc value of A_{OL} in dB. thus the freq. f_1 is called "corner freq" (or) "center/break freq."

(iii) for the freq $f >> f_1$

the gain roles of at a rate of -20dB for decay.

→ the magnitude response is



→ The Gain is deducted w.r.t frequency is called "Roll off"

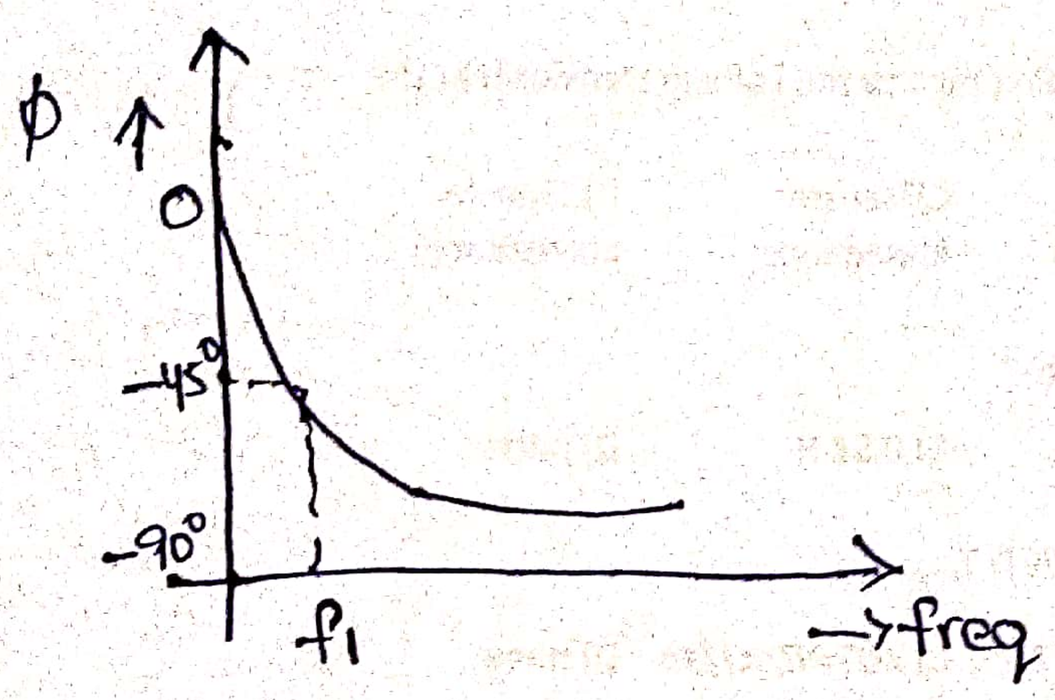
→ It can further we can seen from the phase chorac-
-eristics.

ϕ is 0 at $f=0$

ϕ is $-45°$ at $f=f_1$

ϕ is $-90°$ at $f=\infty$

the phase characteristics is shown below



→ the voltage transfer function in S. domain can be written as

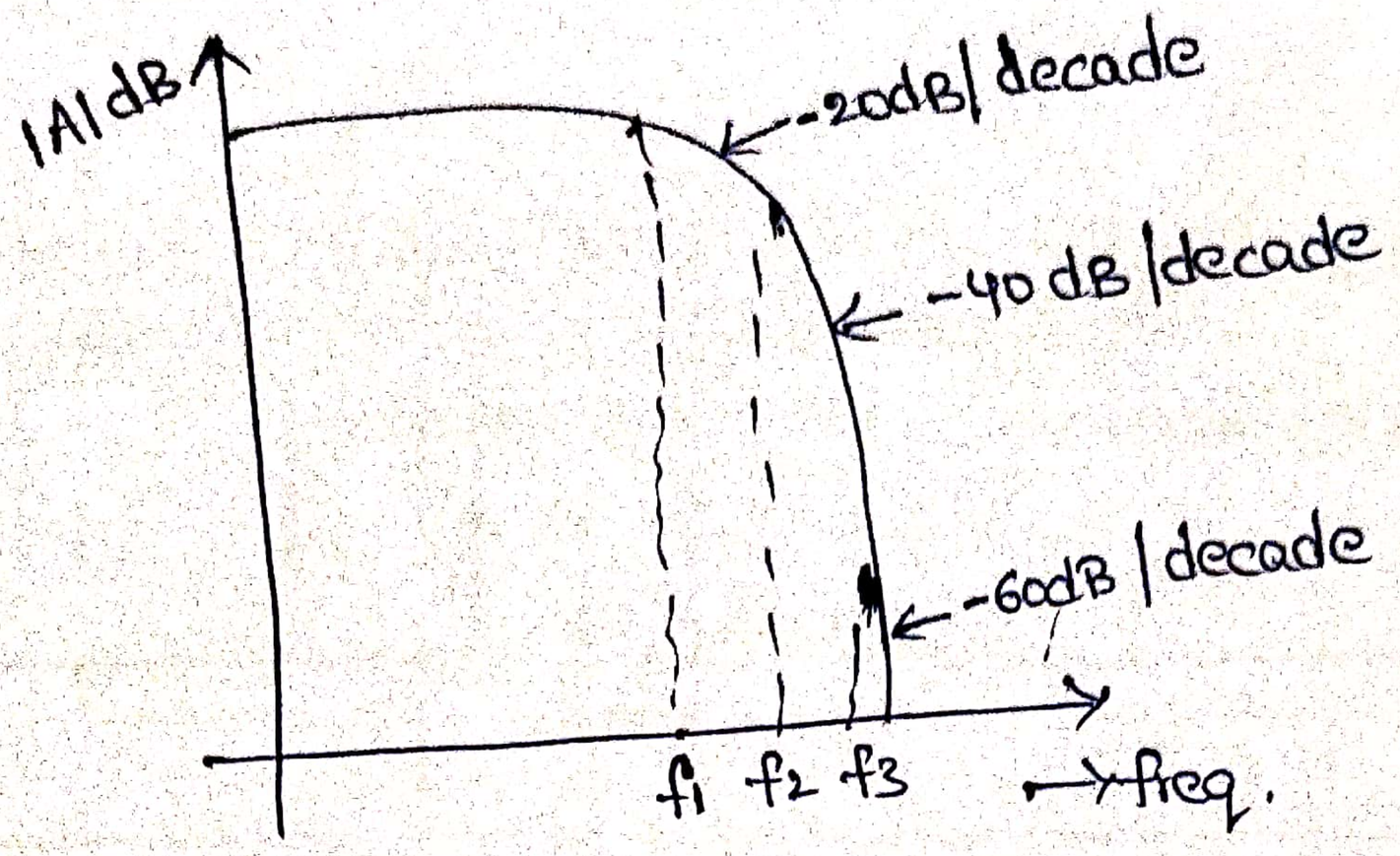
$$A = \frac{A_{OL}}{1 + j\, f/f_1} = \frac{A_{OL}}{1 + \frac{j\omega}{\omega_1}}$$

the S-domain $s = j\omega$

$$\therefore A = \frac{A_{OL} \cdot \omega_1}{\omega_1 + s}$$

→ A practical op-Amp has no. of stages and each stage a capacitive component that transfer function of an op-Amp with 3 break frequency can be assumed as.

$$A = \frac{A_{OL}\ \omega_1\ \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$



Slew Rate :-

The slew rate is defined as the minimum rate of change of o/p voltage with time. Usally the slew rate is expressed in V/μs and is given by.

$$\text{slew rate}, S = \left.\frac{dV_o}{dt}\right|_{max}$$

* The slew rate is caused due to limited charging rate of the compensating capacitor and current limiting.

* saturation of internal stages of an op-amp when a high freq large amplitude signal is applied.

* The interral capacitor voltage can not changes instaneously and is given by,

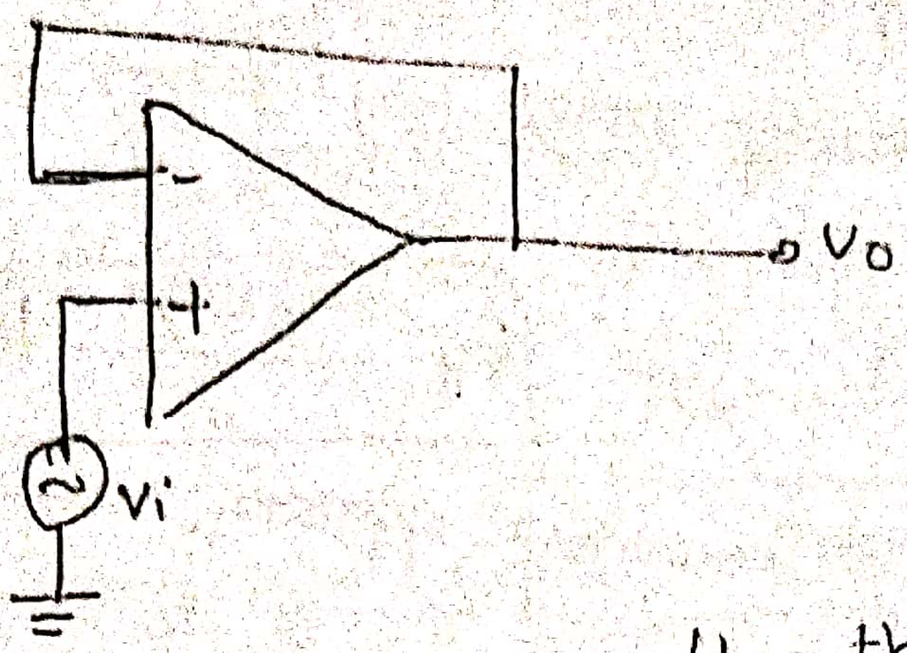
$$\frac{dV_c}{dt} = \frac{I}{C}$$

* For large charging rate capacitor should be small (or) charging current should be large. Hence the slew rate for the op-amp whose maximum internal capacitor charging current is known can be obtained as.

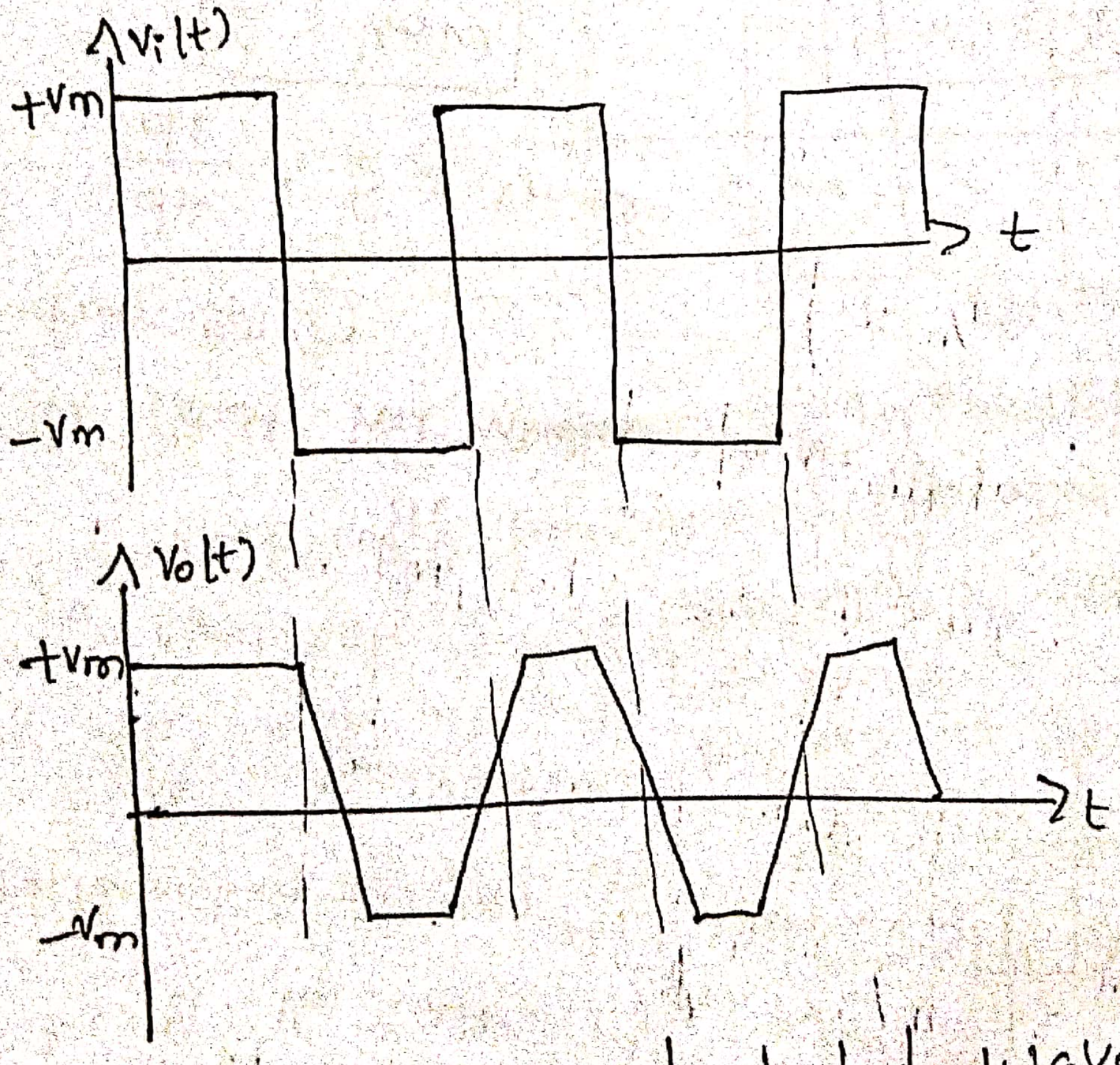
$$S = \frac{I_{c\,max}}{C}.$$

Effect of Slew rate :-

Consider a circuit using op. Amp having unity (16) gain as shown below



→ If the i/p is square wave then the o/p has to be square wave but this is observed for certain frequency of i/p due to slew rate of an op-Amp for a particular i/p frequency o/p gets distorted is shown below



→ Then observing such a distorted waveform on CRO then slew rate can be obtained as

$$S = \frac{\Delta V_o}{\Delta t} V \mid sec$$

Slew Rate Equation :-

Consider the unity gain op. Amp ckt with Pure Sinusoidal i/p the o/p must be same as i/p

$$V_i = V_m \sin \omega t \quad \text{---} (1)$$

$$V_o = V_m \sin \omega t \quad \text{---} (2)$$

differentiate (2) w.r.t 't' then we get

$$\frac{dv_o}{dt} = V_m \cos \omega t \, (\omega) \quad \text{---} (3)$$

The slew rate is defined as

$$S = \frac{dv_o}{dt}\Big|_{max}$$

The $\cos \omega t$ has maximum value is "1"

from Eqn (3)

$$\frac{dv_o}{dt} = S = V_m \omega$$

$$\boxed{S = V_m \omega}$$

$$\boxed{S = 2\pi f_m \omega \ V/sec}$$

→ This is the required Slew rate Equation for distorted free o/p

→ The maximum allowable frequency f_m can be obtained as

$$\boxed{f_m = \frac{S}{2\pi V_m} \ Hz}$$

→ This is also called full Power Bandwidth of the op Amp

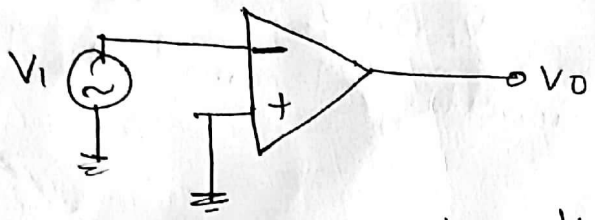
the V_m is Peak of the o/p waveform

Open loop Configuration of OP-Amp :-

In open loop Configuration of op-Amp is operated in 3 modes they are

1. Inverting op-Amp
2. Non inverting OP-Amp
3. Differential mode Configuration.

1. Inverting OP-Amp :-



To operate op-Amp in inverting mode of operation the non-inverting terminal should be grounded and the i/p is applied to the inverting terminal of op-Amp

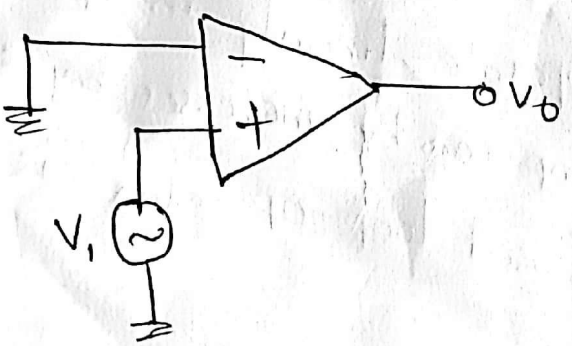
$$V_o = -A_{OL} \cdot V_d$$

$$= A_{OL}(V_2 - V_1)$$

$$= A_{OL}(0 - V_1)$$

$$\boxed{V_o = -A_{OL} V_1}$$

2. Non-Inverting terminal



→ To operate the op-amp in non inverting mode of operat the inverting terminal should be grounded and the i/p sign

The o/p voltage is given by

$V_o = A_{OL} \cdot V_d$

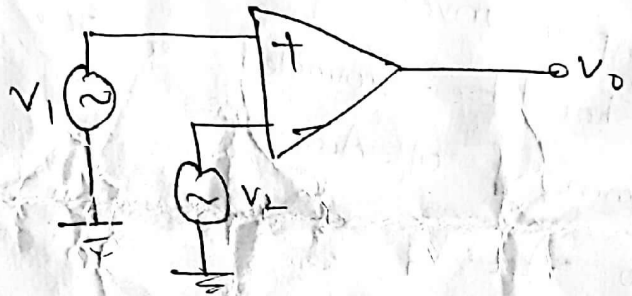
$= A_{OL}(0 + V_1)$

$$\boxed{V_o = A_{OL} V_1}$$

→ from the above Eqn it is clear that the o/p signal is Exactly in phase w.r.t the i/p signal.

3. Differential mode operation :-

To operate the op-amp in differential mode Configuration 2 signal sources V_1 and V_2 are applied to the non-inverting terminal and inverting terminal of op-Amp respectively



$V_o = A_{OL} \cdot V_d$

The o/p voltage is given by

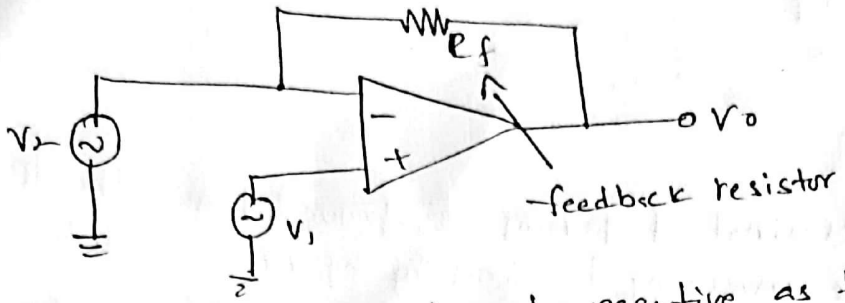
$$\boxed{V_o = A_{OL}(V_1 - V_2)}$$

Closed loop operation :-

op-Amp Cannot operate linearly in open-loop mode but the utility of an op-Amp Can be increases by operating it in closed loop mode. The closed loop operation is possible with the help of feedback

→ In the linear applications of op-amp is always used with -ve feedback. The -ve feedback helps in Controlling gain which other

noise voltage at the i/p terminal. The feedback is provided by adding a resistor called feedback resistor as shown in fig:



→ The feedback is said to be negative as the feedback resistor connects the o/p to the inverting i/p terminal of the op-Amp. The gain resulting with feedback is called closed loop gain of the op-Amp due to feedback resistance is a reduction in the gain.

→ The closed loop gain is much less than the open loop gain

Advantages of -ve feedback :-

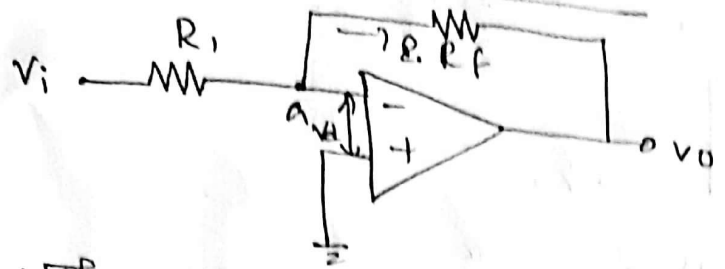
1. It reduces the gain & makes it controllable.
2. It reduces the possibility of distortion
3. It increases the Bandwidth i.e frequency of operation.
4. It increases the i/p resistances of op-Amp
5. It decreases the o/p resistances of op-Amp.
6. It reduces the effects of temperature, Power supply gain of the circuit

Modes of operation in closed loop Configuration :-

In closed loop Configuration there are 3 possibilit modes of operation. They are

1. Inverting mode of operation
2. Non inverting mode of operation
3. differential mode of operation

Inverting Operational Amplifier



→ The non-inverting terminal of op.Amp is grounded and the i/p signal V_i is applied to the inverting terminal of op Amp through the resistance R_i

→ In order to achieve the -ve feedback the feedback resistance R_f is connected b/w v_o to the inverting terminal of the op-Amp.

Circuit Analysis:-

Now we need to derive the expression for closed loop gain

i.e $A_{CL} = \frac{V_o}{V_i}$

Apply nodal Analysis at node 'a'

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_f} = 0 \quad \text{---(1)}$$

due to virtual ground Concept $V_a = 0$ ---(2)

Sub (2) in (1)

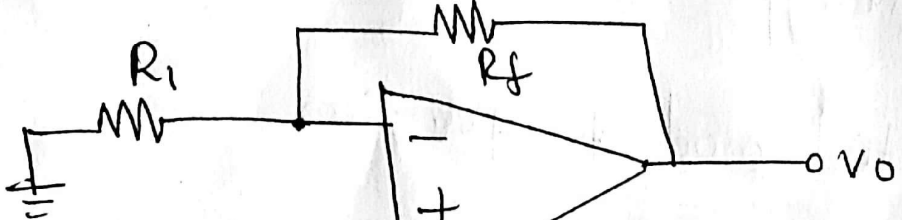
$$\frac{-V_i}{R_1} - \frac{V_o}{R_f} = 0$$

$$\frac{V_o}{R_f} = \frac{-V_i}{R_1}$$

$$\frac{V_o}{V_i} = \frac{-\frac{1}{R_1}}{\frac{1}{R_f}} = -\frac{R_f}{R_1}$$

$$\boxed{A_{CL} = \frac{-R_f}{R_1}}$$

Non-Inverting OP-Amp:-



→ The Signal source is Connected to the non-Inverting terminal of Op-Amp. and the -ve terminal is kept grounded through resistance R_i.

→ To achieve the -ve feedback the feedback resistor R_f is Connected b/w V_0 and inverting terminal of the Op-Amp.

Circuit Analysis :-

Apply nodal eqn at node 'a'

$$\frac{V_a}{R_1} + \frac{V_a - V_0}{R_f} = 0 \quad \text{---} (1)$$

$V_d = 0$, the differential voltage of op-amp $V_d = 0$ the voltage across node a is also equals to zero

$$V_a = V_i \quad \text{---} (2)$$

(2) in (1)

$$\frac{V_i}{R_1} + \frac{V_i - V_0}{R_f} = 0$$

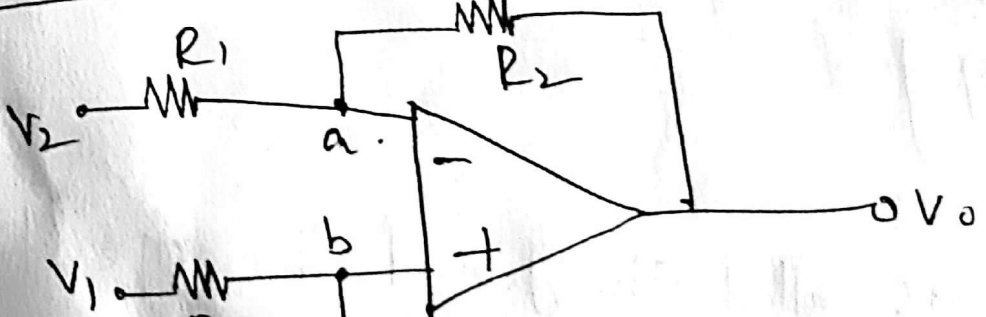
$$V_i \left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_0}{R_f}$$

$$\frac{V_0}{V_i} = \frac{R_1 + R_f}{R_1}$$

$$\boxed{A_{CL} = 1 + \frac{R_f}{R_1}}$$

→ The gain of the non-Inverting Op. Amp is Either Unity (or) greater than Unity is given by Proper adjustment of resistance (R_f and R_1)

3: Differential operational Amplifier :-



→ The signal source V_2 is connected to the inverting terminal of the op-Amp through the resistance R_1 and signal source V_1 is connected to the non-inverting terminal of the op-amp through resistance R_1 to achieve -ve feedback the feedback resistor R_2 is connected b/w V_o and inverting terminal of op-Amp.

Circuit Analysis

Apply nodal Analysis at node 'a'

$$\frac{V_a - V_2}{R_1} + \frac{V_a - V_o}{R_2} = 0 \quad \text{---(1)}$$

Apply nodal analysis at node 'b'

$$\frac{V_b - V_1}{R_1} + \frac{V_b}{R_2} = 0 \quad \text{---(2)}$$

for op-Amp the differential voltage must be equals to zero

i.e $V_d = 0$ for that $V_a = V_b$

(2) $\Rightarrow$ $\frac{V_a - V_1}{R_1} + \frac{V_a}{R_2} = 0$

$$V_a\left[\frac{1}{R_1} + \frac{1}{R_2}\right] = \frac{V_1}{R_1} \quad \text{---(3)}$$

(1) $\Rightarrow$ $V_a\left[\frac{1}{R_1} + \frac{1}{R_2}\right] = \frac{V_2}{R_1} + \frac{V_o}{R_2}$ ---(4)

Sub (3) in (4)

$$\frac{V_1}{R_1} = \frac{V_2}{R_1} + \frac{V_o}{R_2}$$

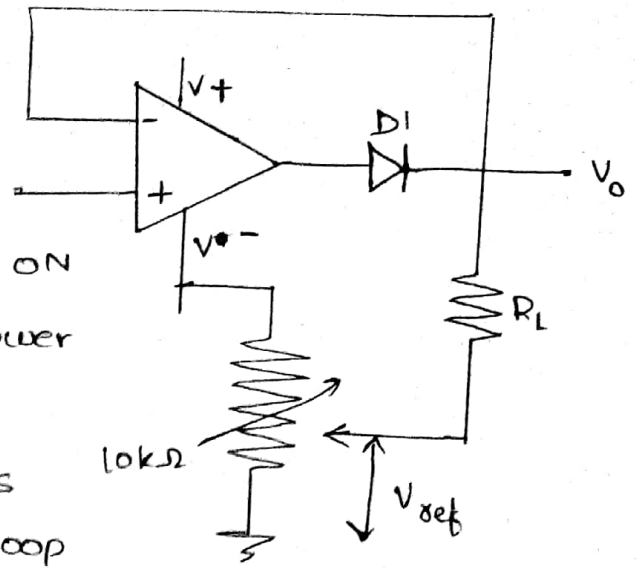
$$\frac{V_o}{R_2} = \frac{V_1 - V_2}{R_1}$$

$$\boxed{V_o = \frac{R_2}{R_1}[V_1 - V_2]}$$

→ The term of $\frac{R_2}{R_1}$ is called the gain of the operational

3) Negative clipper with positive reference voltage:-

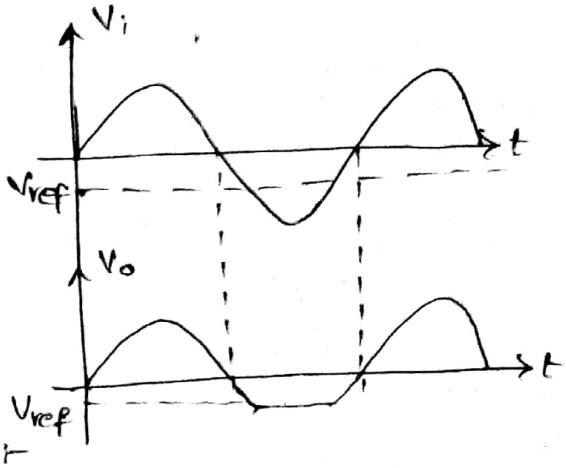
It clips the negative half cycle of input signal. The clipping level is determined by the reference voltage.



i) when $V_i < V_{ref}$, the diode D_1 is ON the op-amp works as voltage follower and o/p, $V_o = V_i$ (till $V_i \leq V_{ref}$)

ii) when $V_i > V_{ref}$, the diode D_1 is off, the op-amp operates in open loop

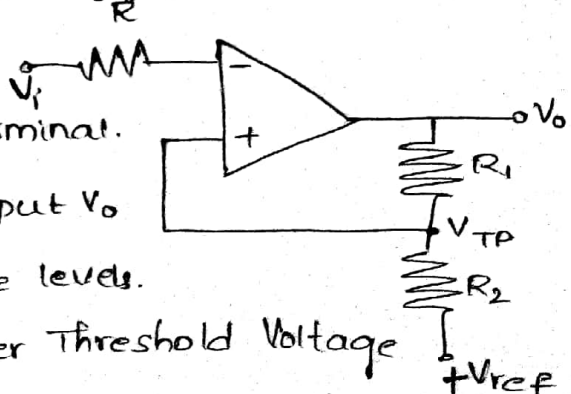
$V_o = V_{ref}$



Regenerative Comparator (Schmitt trigger):-

If positive feedback is added to the comparator circuit, gain can be increased greatly.

The circuit is known as schmitt trigger. The input voltage is applied to the (-) input terminal & feedback voltage at the (+) input terminal.



The input voltage V_i triggers the output V_o every time it exceeds certain voltage levels. These voltage levels are called Upper Threshold Voltage (V_{UTP}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these threshold voltages ie, $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Apply nodal analysis at V_{TP},

$$\frac{V_{TP} - V_{ref}}{R_2} + \frac{V_{TP} - V_o}{R_1} = 0$$

$$V_{TP}\left[\frac{1}{R_1} + \frac{1}{R_2}\right] = \frac{V_o}{R_1} + \frac{V_{ref}}{R_2}$$

$$V_{TP} = \frac{V_o R_2 + V_{ref} R_1}{R_1 R_2} \cdot \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{TP} = \frac{V_o R_2}{R_1 + R_2} + \frac{V_{ref} R_1}{R_1 + R_2}$$

There are two types of triggering points,

Upper triggering point, $V_i > V_{UTP}$, $V_o = -V_{sat}$

lower triggering point, $V_i < V_{LTP}$, $V_o = +V_{sat}$

for upper triggering point,

If $V_i > V_{UTP}$, $V_o = -V_{sat}$

$$V_{UTP} = \frac{R_1 V_{ref}}{R_1 + R_2} - \frac{V_{sat} \cdot R_2}{R_1 + R_2}$$

If $V_i < V_{UTP}$, $V_o = +V_{sat}$

$$V_{UTP} = \frac{R_1 V_{ref}}{R_1 + R_2} + \frac{V_{sat} \cdot R_2}{R_1 + R_2}$$

for lower triggering point,

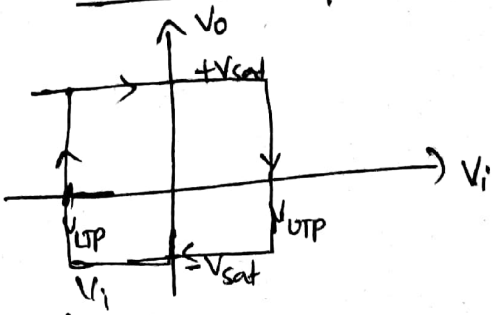
If $V_i > V_{LTP}$, $V_o = -V_{sat}$

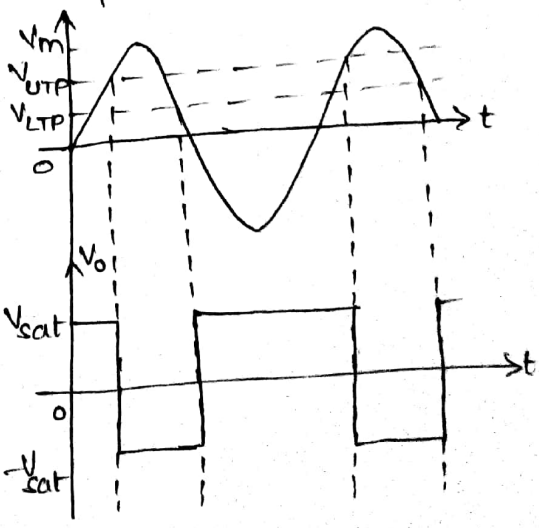
$$V_{LTP} = \frac{R_1 V_{ref}}{R_1 + R_2} - \frac{V_{sat} R_2}{R_1 + R_2}$$

If $V_i < V_{LTP}$, $V_o = +V_{sat}$

$$V_{LTP} = \frac{R_1 V_{ref}}{R_1 + R_2} + \frac{V_{sat} R_2}{R_1 + R_2}$$

Hysteresis curve / Backlash



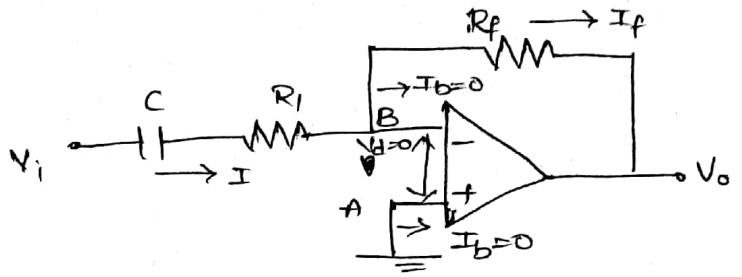


The upper triggering voltage is always greater than lower triggering voltage i.e., $V_{UTP} > V_{LTP}$

AC Amplifiers:- Inverting and Non-Inverting amplifiers responds to both ac and dc signals.

→ One wants to allow only ac signals and blocks dc signal. This is provided by "AC Amplifiers". This is achieved by using an AC amplifier with a coupling capacitor.

Inverting AC Amplifier:- consider an ideal op-amp $I_b=0$, $V_d=0$



capacitor blocks dc components and R_1C forms 3dB frequency

since $V_d=0$

$$V_B-V_A=0 \Rightarrow V_A=V_B=0$$

Apply KCL at node B., $I=I_1$

$$\frac{V_i}{R_1+\frac{1}{j\omega C}} = \frac{-V_o}{R_f}$$

$$\frac{V_o}{V_i} = \frac{-R_f}{R_1+\frac{1}{j\omega C}}$$

$$\frac{V_o}{V_i} = \frac{-R_f \cdot j\omega C}{R_1\left(\frac{1}{R_1}+j\omega C\right)}$$

To allow frequency 'c' value must be high.

$$\frac{V_o}{V_i} = \frac{-R_f}{R_1} \Rightarrow \text{In this } V_i \text{ is only ac signal.}$$

In s-domain, $s=j\omega$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_f}{R_1+\frac{1}{sC}}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_f sC}{1+R_1 sC}$$

$$= \frac{-R_f}{R_1}\left[\frac{s}{s+\frac{1}{R_1C}}\right]$$

where $\omega_L = \frac{1}{R_1C}$

Now, $\frac{V_o(s)}{V_i(s)} = \frac{-R_f}{R_1}\left(\frac{s}{s+\omega_L}\right)$

$s = j\omega$

$$\frac{V_o}{V_i} = \frac{-R_f}{R_1}\left(\frac{j\omega}{j\omega+\omega_L}\right)$$

$$= \frac{-R_f}{R_1}\cdot\frac{1}{\omega_L}\left(\frac{j(\omega/\omega_L)}{j(\omega/\omega_L)+1}\right)$$

Now, $\frac{V_o}{V_i} = \frac{-R_f}{R_1}\left[\frac{j(f/f_L)}{1+j(f/f_L)}\right]$

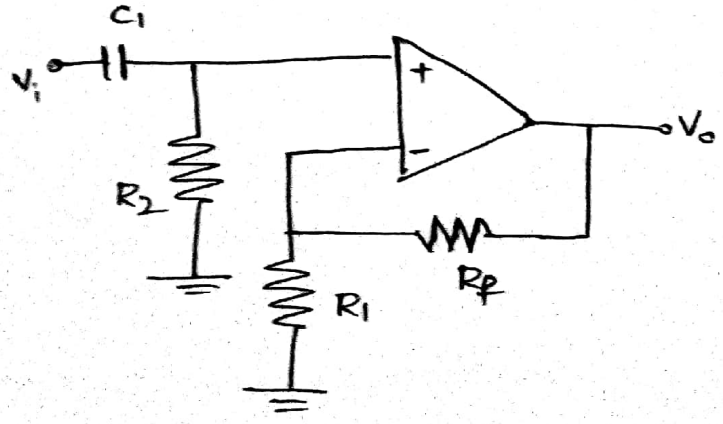
At frequency $f=f_L$, the corresponding gain is given by

$$\frac{V_o}{V_i} = \frac{-R_f}{R_1}\left[\frac{j}{1+j}\right]$$

Now $\left|\frac{V_o}{V_i}\right| = \frac{R_f}{\sqrt{2}R_1}$

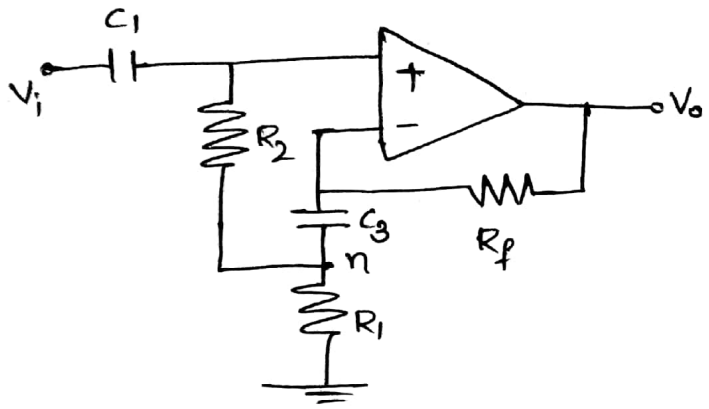
→ Thus from above equation, we can conclude that the magnitude of gain is reduces to 3 dB from its highest value.

Non-Inverting A.C Amplifier:-



→ Hence resistance R_2 is added to provide flow of dc component to the ground however, this reduces the overall i/p impedance of the amplifier which now becomes approximately R_2.

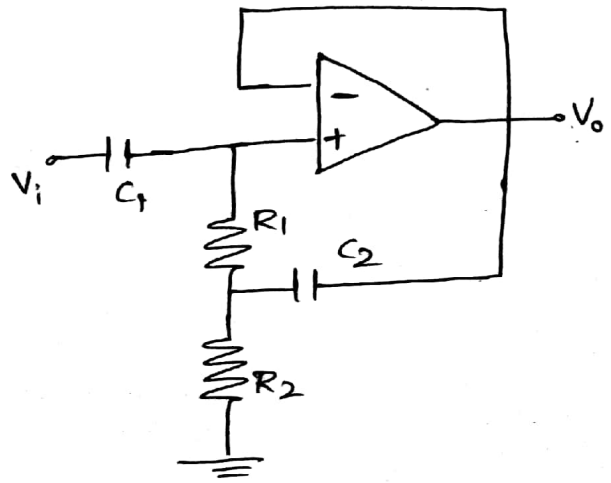
→ The problem of low i/p impedance is eliminated by connecting a capacitor C_3 as shown in the below figure.



→ Capacitor C_3 is large enough to act as short circuit to AC signals.

→ +ve terminal and node 'n' will be at the same potential, so that R_2 carriers almost no current. Hence, the circuit will have extremely high i/p impedance

AC voltage follower (AC voltage Buffer):-



→ This circuit used as a buffer to connect a high impedance signal source and a low impedance load which may be capacitive

→ the capacitor C_1 and C_2 are choosen high so that they are short circuited at all frequencies of operation.

→ The resistors R_1 and R_2 provide a path for dc input current into the non-inverting terminal.

→ The capacitor C_2 acts as a boost strapping capacitor and connects the resistance R_1 to the o/p terminal for AC operation

→ Hence, the i/p resistance of that source sees is approximately $\frac{R_1}{1-A_{CL}}$ (according to Miller's theorem)

∴ The circuit is voltage follower $A_{CL}=1$

$$\text{i/p impedance} = \frac{R_1}{1-1}$$

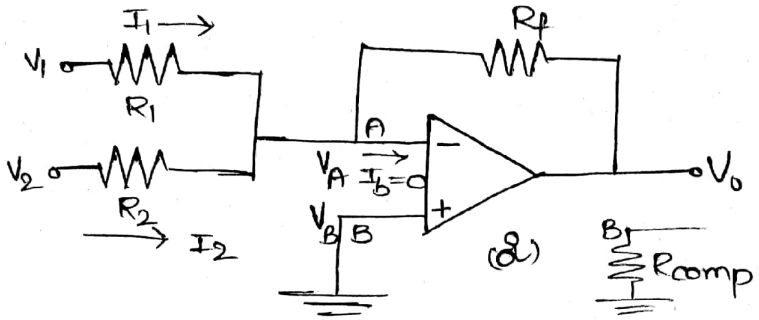
$$= \infty \Rightarrow \text{very high.}$$

Applications of op-amp:-

1) Voltage follower
2) Summing amplifier
   a) Inverting summing amplifier
   b) Non-Inverting summing amplifier
   c) subtractor.

2) Summing amplifier:-

a) Inverting summing amplifier



$V_A = 0$ (By virtual ground concept)

Apply nodal analysis, KVL at node A,

$$\frac{V_A - V_0}{R_f} + \frac{V_A - V_1}{R_1} + \frac{V_A - V_2}{R_2} = 0$$

$$-\frac{V_0}{R_f} - \frac{V_1}{R_1} - \frac{V_2}{R_2} = 0$$

$$V_0 = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

If $R_1 = R_2 = R_f = R$ then it is adder.

if $R_1 = R_2 = R$ and $R \leq R_f$ then it is an inverting amplifier.

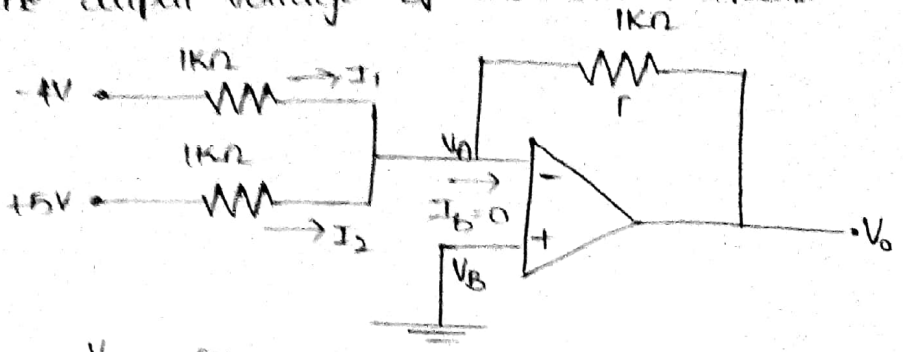
$R_1 = R_2 = R_f = R \Longrightarrow V_0 = -(V_1 + V_2) \Rightarrow$ Adder.

$R_1 = R_2 = R$ and $R_f > R$ then $V_0 = -\frac{R_f}{R_1}(V_1 + V_2)$

↳ Inverting Amplifier.

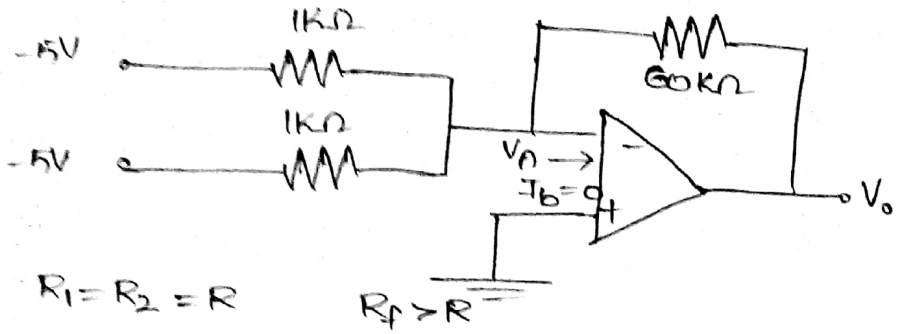
Problems:-

1. Find the output voltage of the below circuit.



$$V_0 = -(V_1 + V_2) = -(-4+5) = -1V$$

2. Find the o/p voltage of the below circuit.

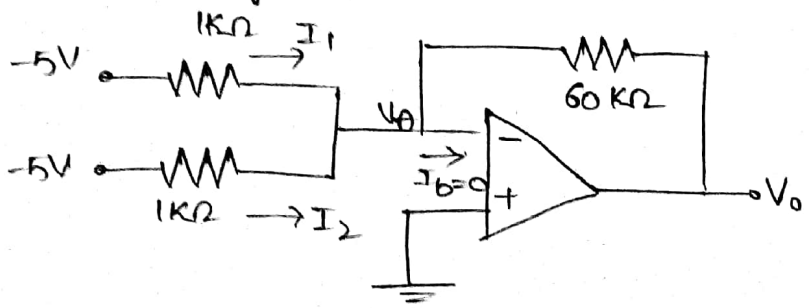


$R_1 = R_2 = R$ $\quad R_f > R$

$$\therefore V_0 = -\frac{R_f}{R_1}(V_1 + V_2) = -\frac{60K}{1K}(-5-5)$$

$$\boxed{V_0 = 600V}$$

3. Find the o/p voltage of below circuit.



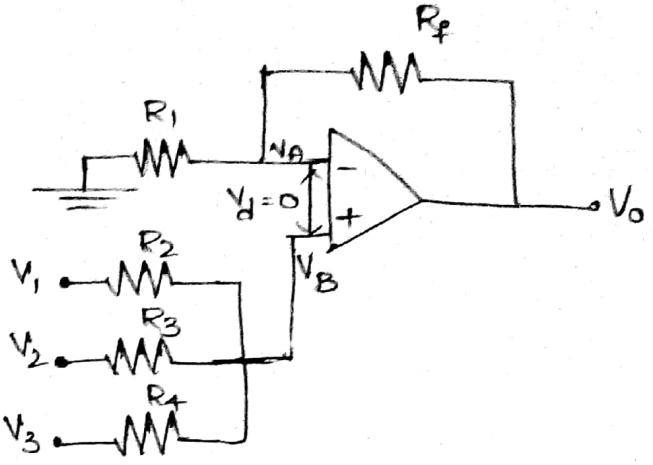
$$\frac{-V_0}{60K} + \frac{5}{1K} + \frac{5}{10K} = 0$$

$$\frac{-V_0 + 300 + 30}{60K} = 0$$

$$\boxed{V_0 = 330V}$$

b) Non-Inverting summing amplifier

when the input signals are added & given to non-inverting terminal of op-amp then it is called as Non-Inverting.



$V_d = V_B - V_A$

$V_d = 0 \Rightarrow V_B = V_A \rightarrow (1)$

Apply voltage division rule,

$$V_A = \frac{V_o \cdot R_1}{R_1 + R_f} \rightarrow (2).$$

Apply nodal analysis at B.,

$$\frac{V_B - V_1}{R_2} + \frac{V_B - V_2}{R_3} + \frac{V_B - V_3}{R_4} = 0$$

$$V_B\left(\frac{1}{R_4} + \frac{1}{R_3} + \frac{1}{R_2}\right) = \frac{V_1}{R_2} + \frac{V_2}{R_3} + \frac{V_3}{R_4}$$

$$V_B = \frac{(V_1/R_2) + (V_2/R_3) + (V_3/R_4)}{1/R_2 + 1/R_3 + 1/R_4} \rightarrow (3).$$

Equate (2) & (3) from (1).,

$$V_o \cdot \frac{R_1}{R_1 + R_f} = \frac{\left(\frac{V_1}{R_2}\right) + \left(\frac{V_2}{R_3}\right) + \left(\frac{V_3}{R_4}\right)}{\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}}$$

$$V_o = \left[\frac{\frac{V_1}{R_2} + \frac{V_2}{R_3} + \frac{V_3}{R_4}}{\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}}\right] \cdot \left(\frac{R_1 + R_f}{R_1}\right)$$

Assume $R_2 = R_3 = R_4 = R$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left[\frac{V_1/R + V_2/R + V_3/R}{1/R + 1/R + 1/R}\right]$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_1 + V_2 + V_3}{R} \times \frac{R}{3}\right)$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left[\frac{V_1 + V_2 + V_3}{3}\right]$$

Assume $1+\frac{R_f}{R_1}=3 \Rightarrow R_f=2R_1$

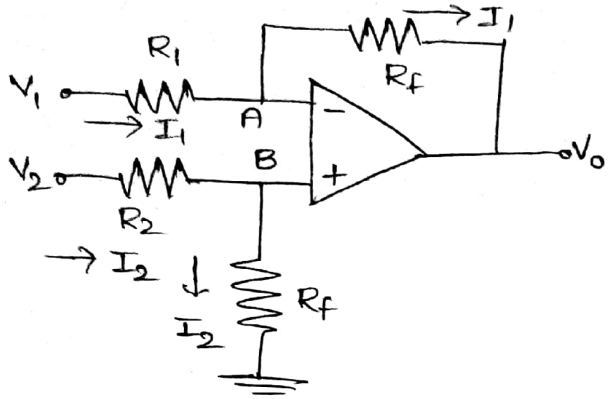
$$V_o=(V_1+V_2+V_3)$$

This equation indicates non-inverting summing amplifier.

c) Subtractor (or) difference amplifier :-

Similar to the summer circuit, the subtraction of two input voltages is possible with the help of op-amp circuit, called subtractor (or) difference amplifier circuit.

→ The circuit diagram is shown below.



The circuit analysis can be done in two ways.

1) Super position Theorem.

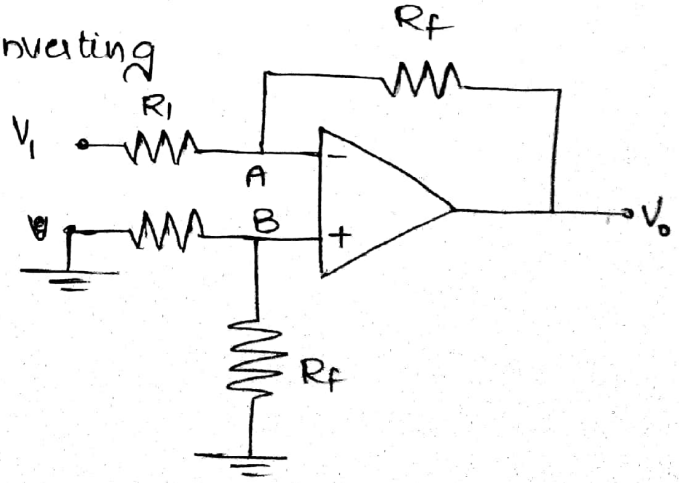
→ In order to find the relation between the inputs & outputs, use super position principle.

According to this, from the circuit the output voltage is given as $V_o = V_{o1} + V_{o2}$. where V_{o1} is the output voltage of the circuit when V_1 is present and V_2 is grounded (0).

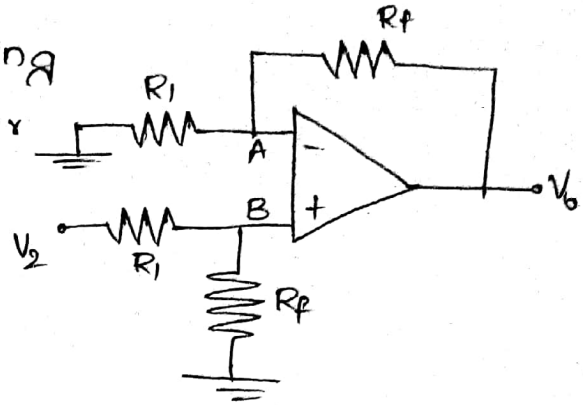
V_{o2} represent the output voltage of the circuit when V_2 is present and V_1 is grounded (0).

case (i) :- V_1 is present and $V_2 = 0$

The circuit looks like inverting amplifier, for inverting amplifier, the output voltage is $V_{o1} = -\frac{R_f}{R_1} V_1$.



Case(ii):- If V_2 is present and $V_1 = 0$.



The circuit looks like non-inverting amplifier, for non-inverting amplifier the output voltage is

$$V_{o_2} = \left(1 + \frac{R_f}{R_1}\right) V_B$$

Apply voltage division rule.,

$$V_B = \frac{V_2 \cdot R_f}{R_1 + R_f}$$

$$V_{o_2} = \left(\frac{R_1 + R_f}{R_1}\right)\left(\frac{V_2 \cdot R_f}{R_1 + R_f}\right)$$

$$V_{o_2} = \frac{V_2 \cdot R_f}{R_1} \rightarrow (2)$$

Total output voltage, $V_o = V_{o_1} + V_{o_2}$

$$V_o = -\frac{R_f}{R_1} \cdot V_1 + \frac{V_2 \cdot R_f}{R_1}$$

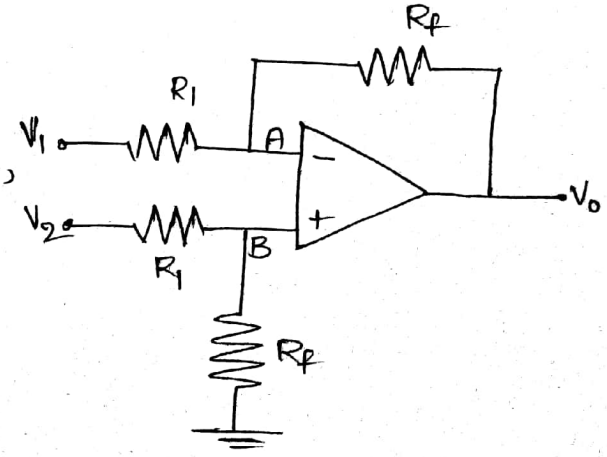
$$\boxed{V_o = +\frac{R_f}{R_1}(V_2 - V_1)}$$

If $R_f = R_1$, $\boxed{V_o = V_2 - V_1}$ ⟹ Subtractor.

$R_f > R_1$, $\boxed{V_o = \frac{R_f}{R_1}(V_2 - V_1)}$ ⟹ Difference amplifier.

2) Nodal Analysis.

$V_d = 0$, $V_B = V_A$



Apply nodal analysis at node A.,

$$\frac{V_A - V_1}{R_1} + \frac{V_A - V_o}{R_f} = 0$$

$$V_A\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = \frac{V_1}{R_1} + \frac{V_o}{R_f}$$

$$V_A = \frac{V_1 R_f + V_o R_1}{R_1 * R_f} \cdot \frac{R_1 * R_f}{R_1 + R_f}$$

$$V_A = \frac{V_1 R_f + V_o R_1}{R_1 + R_f} \rightarrow (1)$$

Apply nodal analysis at node B.,

$$\frac{V_B - V_2}{R_1} + \frac{V_B - V_o}{R_f} = 0$$

$$V_B\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = \frac{V_2}{R_1} + \frac{V_o}{R_f}$$

$$V_B = \frac{V_2 R_f + R_1 V_o}{R_1 \cdot R_f} \cdot \frac{R_1 \cdot R_f}{R_1 + R_f}$$

$$V_B = \frac{V_2 \cdot R_f + V_o R_1}{R_1 + R_f} \rightarrow (2) \Rightarrow V_B = \frac{V_2 \cdot R_f}{R_1 + R_f} \quad (\because V_o = 0)$$

Since $V_A = V_B$., $\frac{V_1 R_f + V_o R_1}{R_1 + R_f} = \frac{V_2 \cdot R_f}{R_1 + R_f}$

$$V_1 R_f - V_2 R_f = -V_o R_1$$

$$R_f (V_1 - V_2) = -V_o R_1$$

$$\frac{R_f}{R_1} = \frac{V_o}{V_2 - V_1}$$

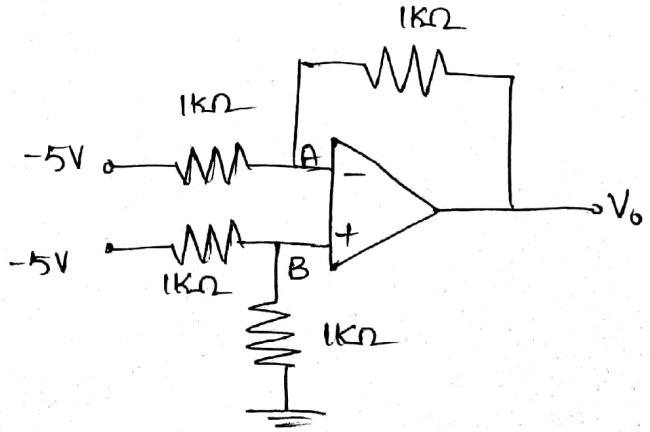
$$\boxed{V_o = \frac{R_f}{R_1}(V_2 - V_1)}$$

problems:-

1. Find the difference voltage for the following circuit.

Sol:-

If resistor values are equal.



$$V_o = V_2 - V_1$$

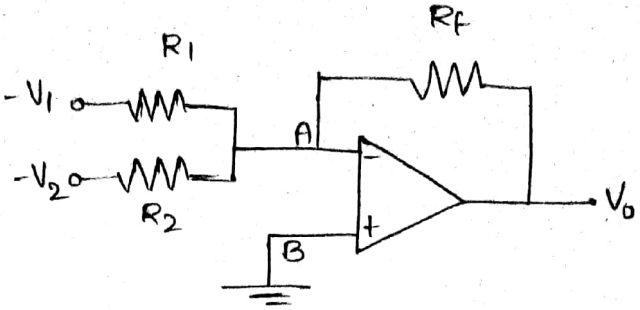
$$V_o = -5 - (-5)$$

$$\boxed{V_o = 0V}$$

2. Design an average circuit with two inputs. (10)

Sol:- case (i):-

consider inverting amplifier



$$V_o = -R_f\left(\frac{-V_1}{R_1} - \frac{V_2}{R_2}\right)$$

$$V_o = R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

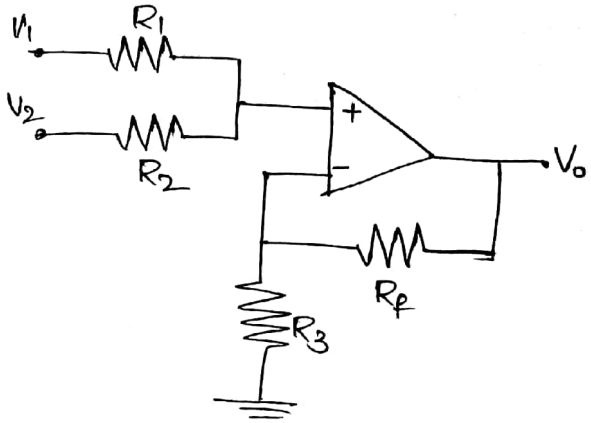
Assume $R_f = 1\Omega$ | $R_f = 1K\Omega$

$R_1 = R_2 = 2\Omega$ | $R_1 = R_2 = 2K\Omega$

$$\boxed{V_o = \frac{V_1 + V_2}{2}}$$

case (ii):- consider non-inverting amplifier

$$V_o = \left(1 + \frac{R_f}{R_3}\right)\left[\frac{(V_1/R_1) + (V_2/R_2)}{1/R_1 + 1/R_2}\right]$$

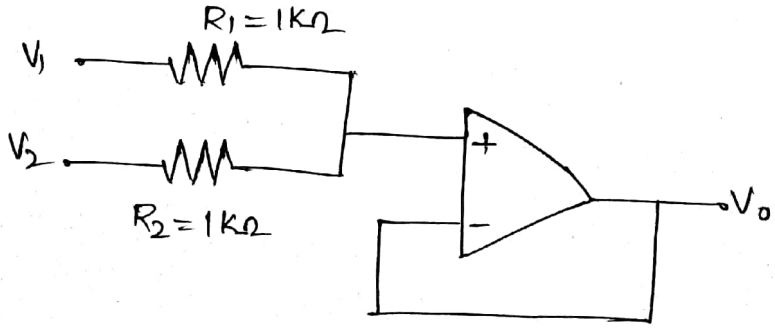


compare with $V_o = \frac{V_1 + V_2}{2}$

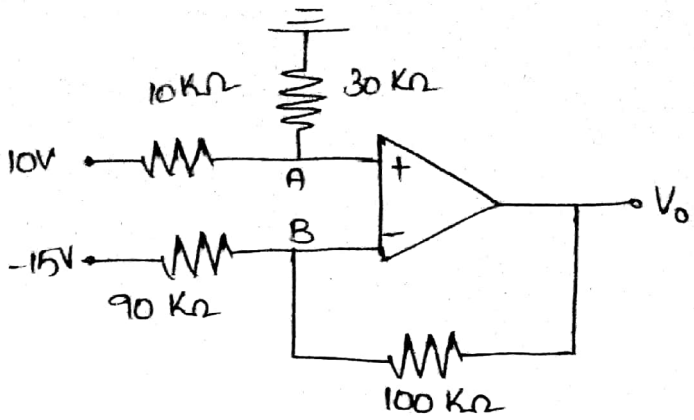
$\left(1 + \frac{R_f}{R_1}\right) = 1$; $R_1 = R_2 = 1K\Omega$

$\frac{R_f}{R_3} = 0 \Rightarrow R_f = 0$

$$\boxed{V_o = \frac{V_1 + V_2}{2}}$$



3. Find the output voltage of below circuit.



Sol:- $V_d = 0 \Rightarrow V_B = V_A$

Apply nodal analysis at node A.,

$$\frac{V_A - 10}{10K} + \frac{V_A - 0}{30K} = 0$$

$$V_A\left(\frac{1}{10K} + \frac{1}{30K}\right) = \frac{10}{10K}$$

$$V_A\left(\frac{1}{10} + \frac{1}{30}\right) = 1.$$

$$V_A = \frac{300}{40} \Rightarrow \boxed{V_A = \frac{30}{4}V}$$

(or) Apply voltage division rule.,

$$V_A = \frac{10 \times 30K}{10K + 30K} = \frac{30}{4}V$$

Apply nodal analysis at node B.,

$$\frac{V_B + 15}{90K} + \frac{V_B - V_o}{100K} = 0$$

$$V_B\left(\frac{1}{90K} + \frac{1}{100K}\right) = \frac{-15}{90K} + \frac{V_o}{100K}$$

$$V_B\left(\frac{100 + 90}{90(100)}\right) = \frac{-15}{90} + \frac{V_o}{100}$$

$$V_B\left(\frac{190}{90(100)}\right) = \frac{V_o}{100} - 0.166$$

$$V_B = \left(\frac{V_o}{100} - 0.166\right)\frac{1}{0.021}$$

$$V_B = \frac{47.33V_o}{100} - 47.33(0.166)$$

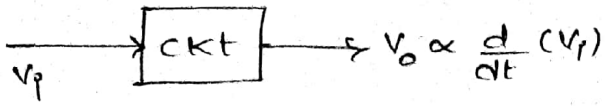
$$V_B = 0.4733V_o - 7.856$$

$$\frac{30}{4} = 0.4733V_o - 7.856$$

$$7.5 + 7.856 = 0.4733V_o$$

$$V_o = \frac{15.356}{0.4733} \Rightarrow \boxed{V_o = 32.44\,V}$$

Differentiator: The circuit which produces the differentiation of the input voltage at its output is called differentiator.



→ The differentiator circuit which doesnot use any active device called passive differentiator.

→ The differentiator circuit which using an active device like op-amp is called an active differentiator.

Ideal op-amp Active differentiator:

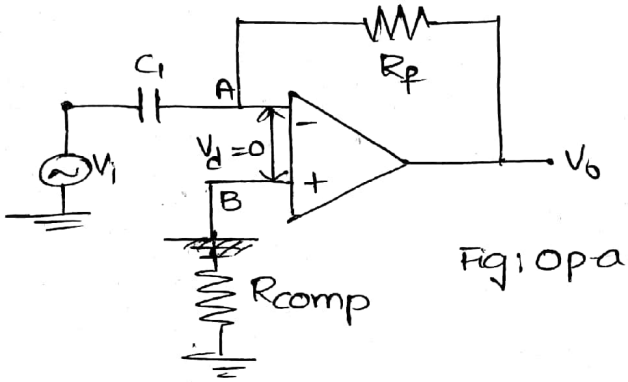


Fig: Op-amp differentiator circuit

The node B is grounded. The node A is also at ground potential.

$$\therefore V_A = 0 \quad (\because V_d = 0)$$

Apply KCL at node A,

$$C_1 \cdot \frac{d}{dt}(V_i + V_A) + \frac{V_A - V_o}{R_f} = 0$$

$$V_A = 0$$

$$C_1 \frac{d(-V_i)}{dt} = \frac{V_o}{R_f}$$

$$-C_1 R_f \frac{dV_i}{dt} = V_o$$

$$\boxed{V_o = -R_f C_1 \frac{dV_i}{dt}}$$

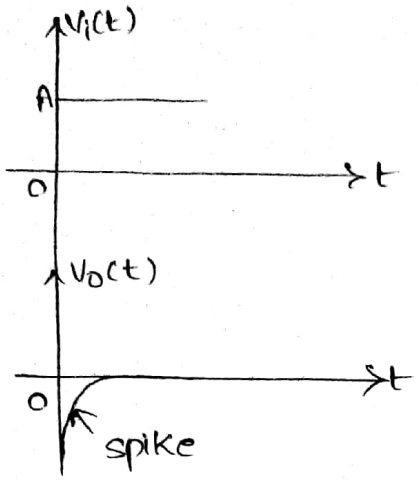
→ The product $R_f C_1$ is called time constant of the differentiator.

→ The negative sign indicates that there is a phase shift of 180° between input and output.

Input-output waveforms of differentiator :-

Assume $R_f C_1 = 1$

i) Step i/p signal :-



$V_i(t) = A$ for $t \geq 0$

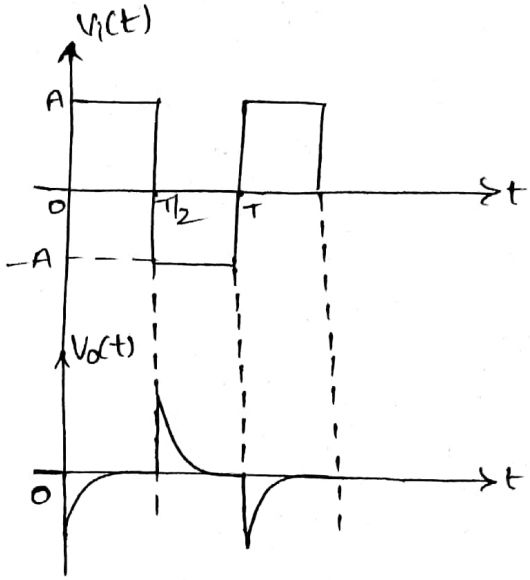
Now $V_o(t) = -\frac{dV_i(t)}{dt} = -\frac{d}{dt}(A)$

→ The step input takes a finite time to rise from 0 to A volts.

→ Due to this finite time, the differentiator output is non-zero but appears in the form of a spike at $t = 0$

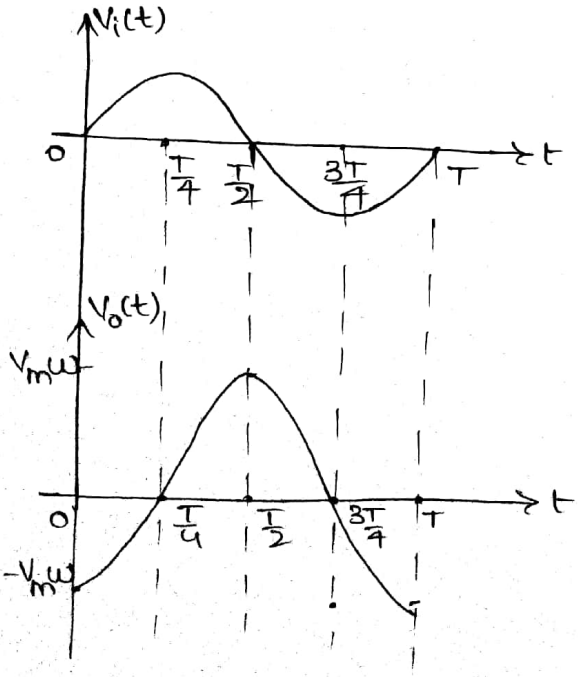
ii) Square input signal :-

$$V_i(t) = \begin{cases} A & 0 < t < T/2 \\ -A & T/2 < t < T \end{cases}$$



→ The differentiator behaves similar to its behaviour to step input.

iii) Sine wave input signal :-



$V_i(t) = V_m \sin \omega t$

Now, $V_o(t) = -\frac{d}{dt} V_i(t)$

$V_o = -\frac{d}{dt}(V_m \sin \omega t) = -V_m \omega \cos \omega t$

At $t = 0$, $V_o(t) = -V_m \omega$

$t = T/4$, $V_o(t) = 0$

$t = T/2$, $V_o(t) = V_m \omega$

Frequency response of Ideal differentiator:

We know that the output voltage of ideal differentiator is given as $V_o(t) = -R_f C_1 \frac{dV_i(t)}{dt}$

Apply laplace transform.,

$$V_o(s) = -R_f C_1 \cdot s V_i(s)$$

Now, Gain of the differentiator is

$$\frac{V_o(s)}{V_i(s)} = -R_f C_1 (j\omega) \quad (\because s = j\omega)$$

$$\therefore A = \frac{V_o(j\omega)}{V_i(j\omega)} = -j R_f C_1 2\pi f$$

To obtain the frequency response, the magnitude of gain is

$$A = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = |-j\omega R_f C_1| = |-j R_f C_1 2\pi f|$$

$$A = 2\pi f R_f C_1$$

let, f_a is the frequency at which gain becomes 0 dB.

$$f_a = \frac{1}{2\pi R_f C_1}$$

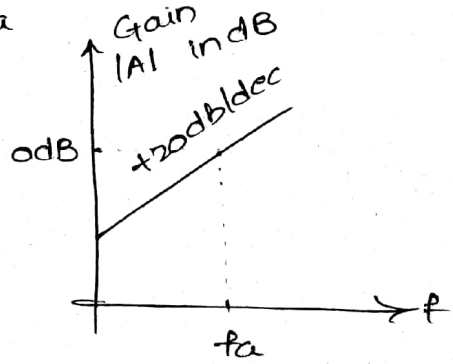
$\therefore$ A can be written as, $A = f/f_a$

$\rightarrow$ Gain in dB $= 20 \log A = 20 \log (f/f_a)$

If $f < f_a$., A in dB is -Ve

$f = f_a$., A in dB = 0

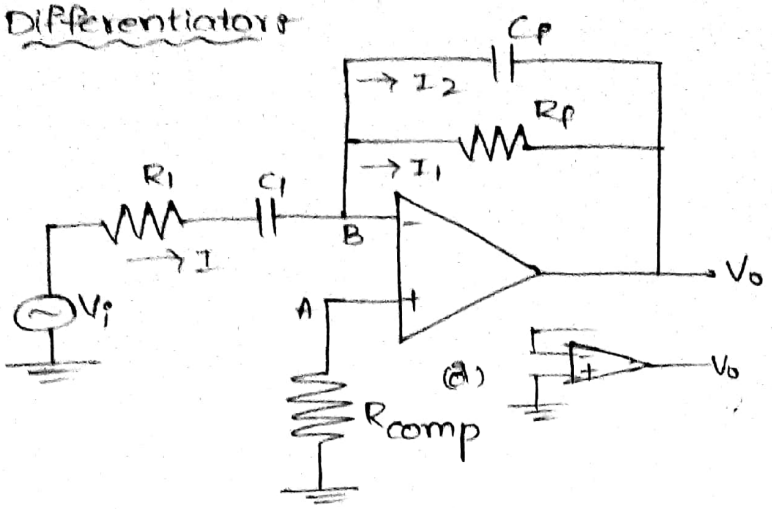
$f > f_a$., A in dB is +Ve



Disadvantages:-

1. Gain in dB increases at higher frequencies, which means the op-amp output goes to saturation means going to oscillate i.e, system is unstable.
2. At very high frequencies, $X_c \simeq 0$. It allows high frequency noise components and also amplifies it greatly.

Practical Differentiator



As the i/p current of op-amp is zero, there is no current at node A.

Then $V_A = 0$

$\therefore V_A = 0 \Rightarrow V_B = 0 \ (\because V_d = 0)$

Circuit Analysis:-

Apply KCL at node B.,

$$I = I_1 + I_2$$

$$\frac{V_i(s)}{R_1 + \frac{1}{sC_1}} = \frac{-V_o(s)}{R_f} - \frac{V_o(s)}{1/sC_f}$$

$$V_o(s)\left[\frac{1}{R_f} + sC_f\right] = \frac{-V_i(s) \cdot sC_1}{1+R_1sC_1}$$

Now, $$\frac{V_o(s)}{V_i(s)} = \frac{-sC_1R_f}{(1+sR_1C_1)(1+sR_fC_f)}$$

If $R_1C_1 = R_fC_f$

$$\frac{V_o(s)}{V_i(s)} = \frac{-sC_1R_f}{(1+sR_1C_1)^2} \rightarrow (1)$$

Here $R_fC_1 >> R_1C_1$ (&) R_fC_f but $R_fC_1 << T$

Now eq.(1) becomes.,

$$V_o(s) = -sR_fC_1 V_i(s) \ (\because \text{denominator is ignored})$$

$$\boxed{V_o(t) = -R_fC_1 \frac{d}{dt} v_i(t)}$$

$\therefore$ It acts as a differentiator.

Frequency Response of practical differentiator:-

W.K.T., $\frac{V_o(s)}{V_i(s)} = \frac{-sC_1R_f}{(1+sR_1C_1)^2}$ $(\because R_1C_1 = R_fC_f)$

put $s = j\omega$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\omega C_1R_f}{(1+j\omega R_1C_1)^2} = \frac{-j2\pi f R_fC_1}{(1+j2\pi f R_1C_1)^2}$$

let $f_b = \frac{1}{2\pi R_1C_1}$; $f_a = \frac{1}{2\pi R_fC_1}$

Now, $$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j(f/f_a)}{(1+j(f/f_b))^2}$$

Now, the magnitude is given as,

$$A = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|\frac{-j(f/f_a)}{(1+j(f/f_b))^2}\right|$$

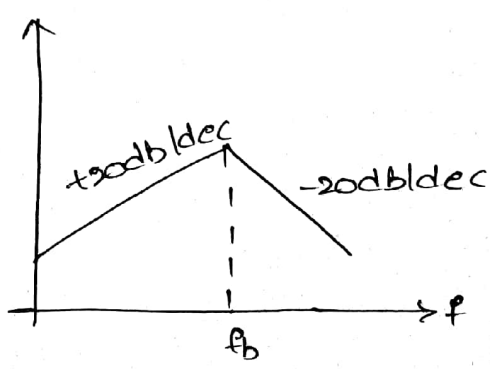
$$A = \frac{(f/f_a)}{\left(\sqrt{1+(f/f_b)^2}\right)^2} = \frac{(f/f_a)}{1+(f/f_b)^2}$$

Now, gain in dB $= 20\log_{10}A = 20\log_{10}\left[\frac{(f/f_a)}{1+(f/f_b)^2}\right]$

W.K.T., $R_fC_1 >> R_1C_1$, we can write $f_a < f_b$

$f > f_b \Rightarrow$ gain decreases

$f < f_b \Rightarrow$ gain increases.



Advantages:-

1. At high frequencies, gain is limited. So, circuit is stable.
2. Due to R_1C_1 and R_fC_f combination, high frequency noise is just reduced.

Design of practical differentiator:

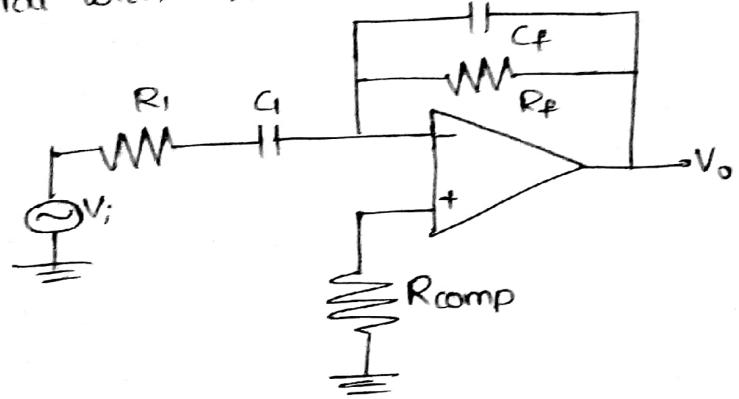
1. Choose f_a as max. frequency of input signal.
2. $f_a = \frac{1}{2\pi R_f C_1}$ choose $C_1 \leq 1\mu F$
3. $f_b > f_a \Rightarrow \boxed{f_b = 10 f_a}$

$$\frac{1}{2\pi R_1 C_1} = 10 \times \frac{1}{2\pi R_f C_1}$$

$$\boxed{R_f = 10 R_1}$$

4. $R_f C_f = R_1 C_1$
5. $R_{comp} = R_1 \| R_f$

problem:- Design practical differentiator which differentiates the i/p sinusoidal with $f_{max} = 200$ Hz.



Sol:- Given $f_a = 200$ Hz, let $C_1 = 1\mu F$

$$\frac{1}{2\pi R_1 C_1} = 200 \Rightarrow R_f = \frac{1}{2\pi \times 200 \times 1\mu} = 795.77\Omega$$

$$f_b = 10 f_a \Rightarrow f_b = 2K\ Hz$$

$$f_b = \frac{1}{2\pi R_1 C_1} \Rightarrow R_1 = \frac{1}{2\pi \times 1\mu \times 2k} = 79.57\Omega$$

$$R_f C_f = R_1 C_1 \Rightarrow C_f = \frac{R_1 C_1}{R_f} = \frac{79.57 \times 1\mu}{795.77}$$

$$C_f = 99.9\,nF$$

$$R_{comp} = R_1 \| R_f = 72.33\Omega$$

8) Design the practical differentiator whose frequency is 1KHz. (14)

Sol: $f_a = 1KHz \Rightarrow f_b = 10(f_a)$

$f_b = 10KHz$

$C_1 = 1\mu F$

$f_a = \frac{1}{2\pi R_f C_1} \Rightarrow 1\times10^{+03} = \frac{1}{2\pi(R_f(1\times10^{-6})}$

$R_f = 159.15\Omega$

$R_i C_1 = R_f C_f$

$C_f = \frac{(15.9)(1\mu)}{159.1}$

$C_f = 9.98\times10^{-8}F$

$R_{comp} = R_1 // R_2$

$= \frac{2529.69}{175}$

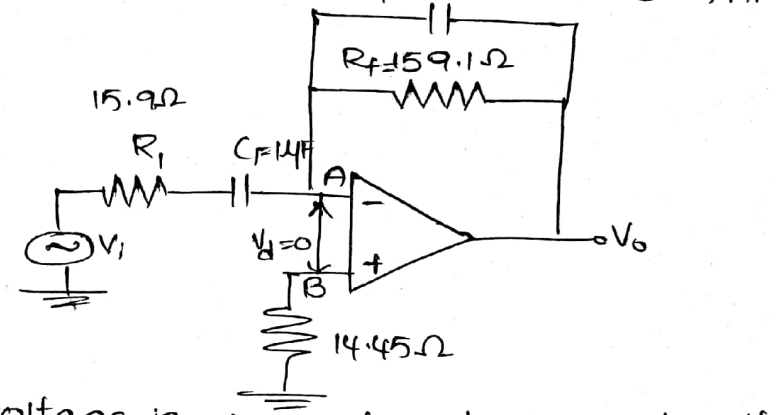
$= 14.45\Omega$

$f_b = \frac{1}{2\pi R_1 C_1}$

$R_1 = \frac{1}{2\pi\times10^{-6}\times10\times10^{3}}$

$R_1 = 15.9\Omega$

$C_f = 9.98\times10^{-8}nF = 0.09nF$



Integrator: The output voltage is the integral of input voltage is referred as integrator.

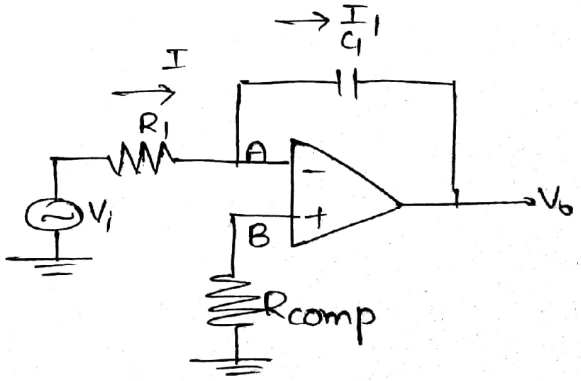
1) passive Integrator

The circuit using passive elements referred as passive Integrator.

2) Active Integrator

The circuit using active elements is referred as active Integrator.

Ideal Integrator (Active) circuit:-



Apply KCL at node A,

$I = I_1$

$\frac{V_i - V_A}{R_1} = \frac{d}{dt}(V_A - V_o)\,C_f$

$V_B = 0 \Rightarrow V_A = 0 \quad (\because V_d = 0)$

$\frac{V_i}{R_i} = -C_f \frac{d}{dt} V_o.$

$V_o = \frac{-1}{R_1 C_f}\int_0^t V_i(t)\,dt \Rightarrow \boxed{V_o = \frac{-1}{R_1 C_f}\int_0^t V_i(t)\,dt}$

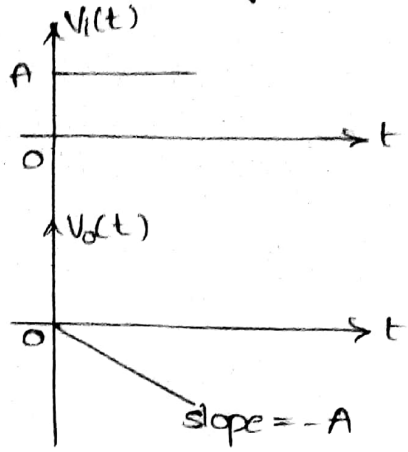
$R_f C_f$ is the time constant of the integrator.

$R_f C_f >> T$

$V_o \propto \int V_i \, dt$ means it acts as basic integrator circuit.

Input & Output Wave-forms:-

1) step input signal.



Assume $R_f C_f = 1$

$$V_i(t) = \begin{cases} A & t \geq 0 \\ 0 & t < 0 \end{cases}$$

Now, $V_o(t) = -\int_0^t V_i(t)\, dt$

$$= -A \int_0^t dt = -A(t)_0^t$$

$$\boxed{V_o(t) = -At}$$

Thus, the o/p wave-form is a straight line with the slope of - A.

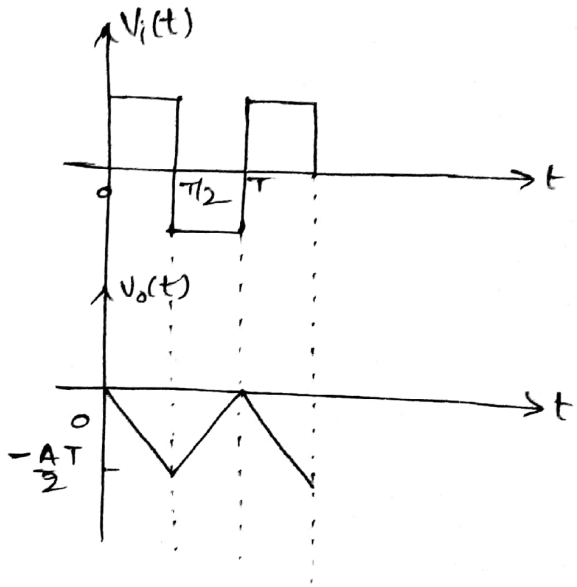
ii) Square wave input signal:-

$$V_i(t) = \begin{cases} A & 0 < t < T/2 \\ -A & T/2 < t < T \end{cases}$$

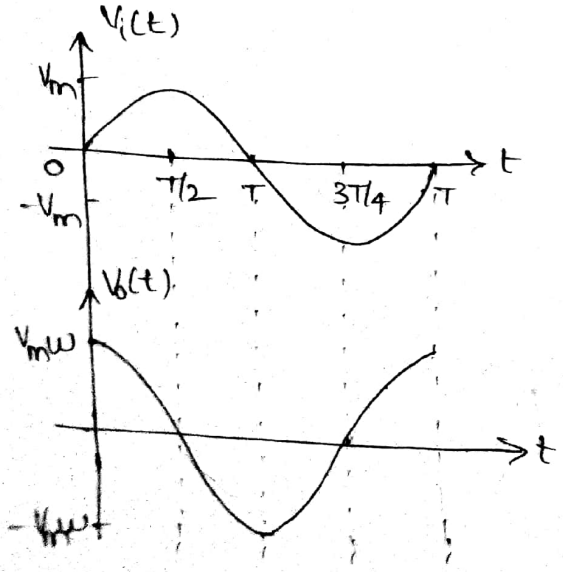
Now, $V_o(t) = -\int_0^t V_i(t)\, dt$

$$= -\left[\int_0^{T/2} A\, dt + \int_{T/2}^{T} -A\, dt \right]$$

$$V_o(t) = \begin{cases} -At & 0 < t < T/2 \\ At & T/2 < t < T \end{cases}$$



iii) Sine wave input signal:-



$V_i(t) = V_m \sin \omega t$

Now, $V_o(t) = -\int V_i(t)\, dt$

$= -\int V_m \sin \omega t \, dt$

$$V_o(t) = \frac{-V_m(-\cos \omega t)}{\omega}$$

$$V_o(t) = \frac{V_m}{\omega} \cos \omega t$$

Frequency Response of Ideal Integrator:-

W.K.T., $V_o = \frac{-1}{R_1 C_f} \int V_i(t)\, dt$

Apply laplace transform, we get

$$V_o(S) = \frac{-1}{R_1 C_f} \cdot \frac{V_i(S)}{S}$$

$$\frac{V_o(S)}{V_i(S)} = \frac{-1}{S R_1 C_f}$$

put $S = j\omega = j 2\pi f$

Now, gain of integrator is $\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1}{R_1 C_f 2\pi f}$

let $f_a = \frac{1}{2\pi R_1 C_f}$

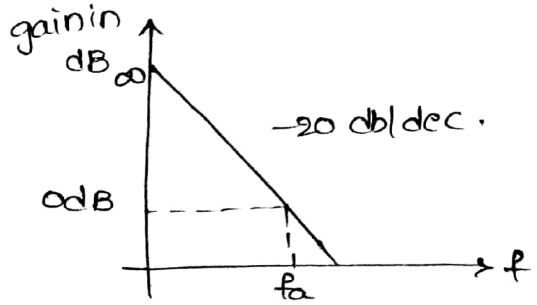
Now gain, $A = \frac{-f_a}{f}$

The magnitude of the gain is $A = \left|\frac{-f_a}{f}\right| = \frac{f_a}{f}$

Gain in dB $= 20 \log (f_a/f)$

At $f = 0 \Rightarrow$ gain in dB $= \infty$

$f = f_a \Rightarrow$ gain in dB $= 0$ dB

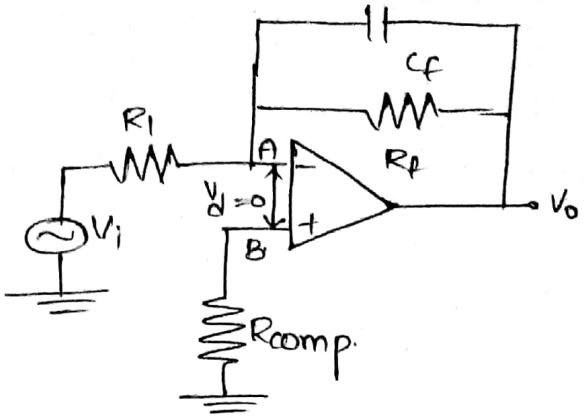


Disadvantages:-

1. For 0Hz $\Rightarrow$ gain is ∞. If i/p is not applied, due to i/p offset voltage, i/p bias current, the o/p is very high (error o/p).
2. If i/p is applied, o/p is not ~~err~~ exact integration of input due to V_{ios} and I_b.
3. Bandwidth is very less. So, it is used as integrator for limited frequencies only.

→ To overcome this, we use practical integrator.

practical Integrator:-



The difference voltage, $V_d = 0$

$V_B = V_A$, $V_A = 0$

-Apply nodal analysis at A,

$$\frac{V_A - V_i}{R_1} + \frac{V_A - V_o}{R_f} + \frac{V_A - V_o}{1/sC_f} = 0$$

Since $V_A = 0$

$$\Rightarrow -V_o\left(\frac{1}{R_f} + sC_f\right) = \frac{V_i}{R_1}$$

$$V_o(s) = \frac{-V_i(s) \cdot R_f}{R_1(1+sC_fR_f)}$$

$$V_o(s) = \frac{-V_i(s)}{\frac{R_1}{R_f}(1+sC_fR_f)}$$

$$V_o(s) = \frac{-V_i(s)}{\frac{R_1}{R_f} + sC_fR_1}$$

consider $R_f >> R_1 \Rightarrow \frac{R_f}{R_1} >> 1 \Rightarrow \frac{R_1}{R_f} << 1$

$$V_o(s) = \frac{-V_i(s)}{1+sC_fR_1}$$

Apply inverse laplace transform.,

$$V_o(t) = \frac{-1}{R_1C_f}\int V_i\, dt$$

Input-Output wave-forms of practical Integrator:-

It is same as ideal integrator.

-frequency Response of practical integrator:-

The output voltage of practical Integrator in s-domain is given as

$$V_o(s) = \frac{-V_i(s)}{\frac{R_1}{R_f} + 1 + sC_fR_1}$$

$$V_o(s) = \frac{-R_f V_i(s)}{R_1(1+sC_fR_f)}$$

$$s = j\omega = j2\pi f$$

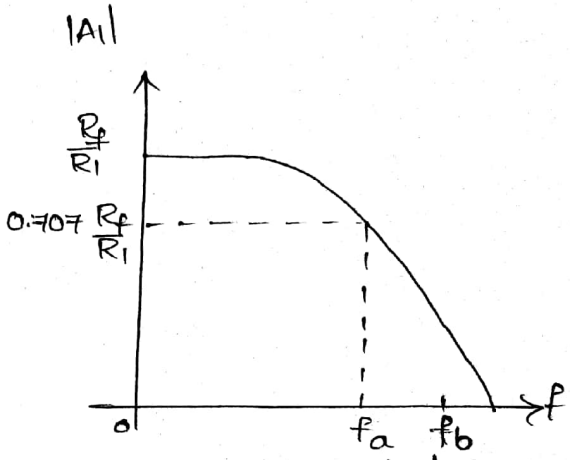
$$A = \frac{V_o(s)}{V_i(s)} = \frac{-R_f}{R_1(1+j2\pi f R_f C_f)}$$

$$f_a = \frac{1}{2\pi R_f C_f} \qquad f_b = \frac{1}{2\pi R_1 C_f}$$

$f_b > f_a$.,

$$A_1 = \frac{-R_f}{R_1(1+j(f/f_a))}$$

$$|A_1| = \frac{(R_f/R_1)}{\sqrt{1+(f/f_a)^2}}$$



$f = 0$., $|A_1| = R_f/R_1 \Longrightarrow$ DC gain

$f = f_a$., $|A_1| = R_f/\sqrt{2}R_1 \Longrightarrow$ 3dB gain

$f \geq f_a$., $|A_1| \Rightarrow$ decreases

$f = \infty$., $|A_1| = 0$

$\longrightarrow$ For pure integrator, gain is straight line. So, it is also called as "Lossy integrator".

Applications:-

1. In analog computers.
2. ADC's
3. In wave shaping circuits.
4. To generate ramp signals.

steps to design practical integrator:-

1. Select f_b as maximum input frequency.
2. As $f_b > f_a$, choose f_b is $10f_a$., $f_b = 10f_a$

$$f_a = \frac{f_b}{10}$$

3. Finding of R_f and R_1., $f_b = 10\, f_a$

$$\frac{1}{2\pi R_1 C_f} = 10 \cdot \frac{1}{2\pi R_f C_f}$$

$$R_f = 10 R_1$$

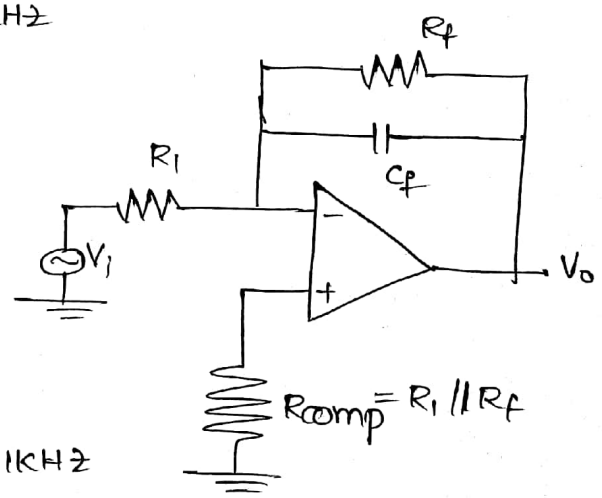
choose $R_1 \leq 10K\Omega$

4. consider $f_b = \frac{1}{2\pi R_f C_f} \Longrightarrow C_f = \frac{1}{2\pi R_f f_b}$

5. $R_{comp} = R_1 // R_f$

problems:-

1. Design lossy integrator with dc gain = 10 which integrates the square input with frequency 10 KHz



Sol:- dc gain = 10

$$20 \log (R_f/R_1) = 10$$

$$R_f = R_1\, 10^{1/2} = 3.16\, R_1$$

let $R_1 = 10K\Omega$., $R_f = 31.6\, K\Omega$

choose $f_a = 10$ KHz; $f_b = \frac{f_a}{10} = 1KHz$

$$\frac{1}{2\pi R_f C_f} = 1K$$

$$C_f = \frac{1}{2\pi (R_f 0K)} = 5.03\, nF$$

$$R_{comp} = R_1 // R_f$$

2) Find the values of R_1 and R_f. Given gain in dB = 40dB & gain is decreased by 3dB at $f = 1.5$ KHz ; $C_f = 0.1\mu F$.

Sol:- At $f = 0$ Hz ., $20 \log \left(R_f / R_1 \right) = 40$

$$\frac{R_f}{R_1} = 100$$

3dB gain., $$37 = 20 \log \left[\frac{100}{\sqrt{1 + (1.5K/f_b)^2}} \right]$$

$$10^{1.85} = \frac{100}{\sqrt{1 + (1.5K/f_b)^2}}$$

$$\boxed{f_b = 1.5 \text{ KHz}}$$ (∵ for checking).

3. Design a practical integrator whose frequency is 10KHz.

Sol:- $f_b = 10$ KHz

$$f_a = \frac{f_b}{10} \Rightarrow f_a = 1 \text{KHz}$$

$$R_f = 10 R_1$$

let $R_1 = 9K\Omega$., $R_f = 10 \times 9 K\Omega$

$$R_f = 90K\Omega$$

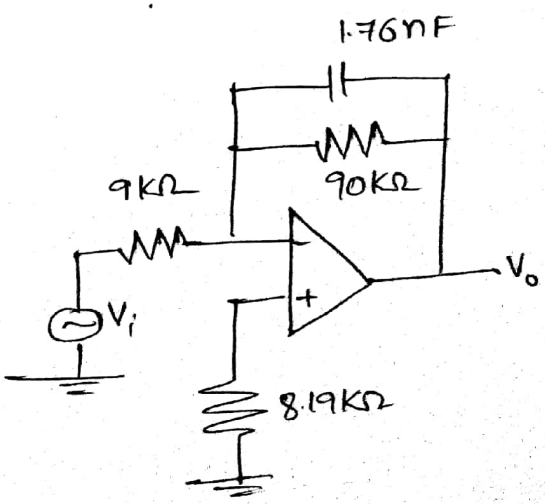
$$C_f = \frac{1}{2\pi R_1 f_b} \Rightarrow C_f = \frac{1}{2\pi \times 100 \times 10^3 \times 9 \times 10^3}$$

$$C_f = 1.76 \text{ nF}$$

$$R_{comp} = R_1 \| R_f = \frac{R_1 \cdot R_f}{R_1 + R_f}$$

$$= \frac{(9 \times 10^3)(90 \times 10^3)}{(9 \times 10^3) + (90 \times 10^3)}$$

$$= 8.19K\Omega$$



4. Find the value of R_1 and R_f of integrator so that the peak gain is 20dB and the 3dB gain from its peak occur at $\omega = 10{,}000$ rad/sec. use a capacitor of value 0.01μF.

Sol:- Given $C_f = 0.01\mu F$

At $f=0 \Rightarrow \omega = 0 \Rightarrow$ dc gain = 20dB

At $\omega = 10{,}000$ rad/sec., 3dB gain = Max. gain − 3dB

= 20dB − 3dB

= 17dB.

$$\text{dc gain} = 20 \log \left(\frac{R_f}{R_1}\right)$$

$$20 = 20 \log_{10}(R_f/R_1)$$

$$1 = \log_{10}(R_f/R_1)$$

$$R_f = 10R_1 \Rightarrow R_1 = \frac{R_f}{10}$$

$$\text{3dB gain} = 20 \log \left(\frac{R_f}{R_1\sqrt{1+\omega^2 R_f^2 C_f^2}}\right)$$

$$17 = 20 \log \left[\frac{R_f}{\frac{R_f}{10}\sqrt{1+(10^4)^2 R_f^2 (0.01\mu)^2}}\right]$$

$$\frac{17}{20} = \log\left[\frac{10}{\sqrt{1+10^8 R_f^2 10^{-16}}}\right]$$

$$0.85 = \log\left(\frac{1}{\sqrt{1+R_f^2 10^{-8}}}\right)$$

$$\log 10 - \log\sqrt{1+R_f^2 10^{-8}} = 0.85$$

$$\frac{1}{2}\log(1+10^{-8}R_f^2) = \frac{3}{20}$$

$$1+10^{-8}R_f^2 = 10^{0.3}$$

$$10^{-8}R_f^2 = 1.99-1$$

$$R_f 10^{-4} = \sqrt{0.99}$$

$$= 0.994$$

$$\boxed{R_f = 9.94\ K\Omega} \Rightarrow \boxed{R_1 = 0.9\ K\Omega}$$

5. The below figure shows a non-inverting circuit. Show that

$$V_o = \frac{1}{RC}\int V_i\,dt$$

Sol:- Apply nodal analysis at node A.,

$$\frac{V_A - V_i}{R} + \frac{V_A - 0}{1/sC} = 0$$

$$V_A\left(\frac{1}{R} + sC\right) = \frac{V_i}{R} \Rightarrow V_A = \frac{V_i}{R}\cdot\frac{R}{1+sC}$$

$$V_A = \frac{V_i}{1+sRC}$$

At node B., $\frac{V_B - 0}{R} + \frac{V_B - V_o}{1/sC} = 0$

$$V_B\left(\frac{1}{R} + sC\right) = \frac{V_o}{1/sC}$$

$$V_B = sC.V_o.\frac{R}{1+sCR} \Rightarrow V_B = \frac{V_o.\,sCR}{1+sCR}$$

$$V_A = V_B$$

$$\frac{V_i}{1+sCR} = V_o.\frac{sRC}{1+sCR}$$

$$V_o = \frac{1}{sRC}V_i$$

Apply inverse laplace transform.,

$$V_o = \frac{1}{RC}\int V_i\,dt.$$

6. Consider the integrator of type lossy whose component values are given as $R_1 = 10K\Omega$, $R_f = 100K\Omega$, $C_f = 10nF$. Determine the lower frequency limit of integration & study the response of input signal.

i) sine wave whose amplitude is 1V & frequency is 5KHz.

ii) step input

iii) Square wave

Sol:- Given $R_1 = 10K\Omega$, $R_f = 100K\Omega$, $C_f = 10nf$

$$f_a = \frac{1}{2\pi R_f C_f} \Rightarrow f_a = \frac{1}{2\pi\times10^5\times10^{-9}\times10}$$

$$f_a = 159.1\ Hz$$

i) Sine wave, Amplitude = 1V frequency = 5 KHz

$\omega = 2\pi f$

$\omega = 2\pi(5K)$

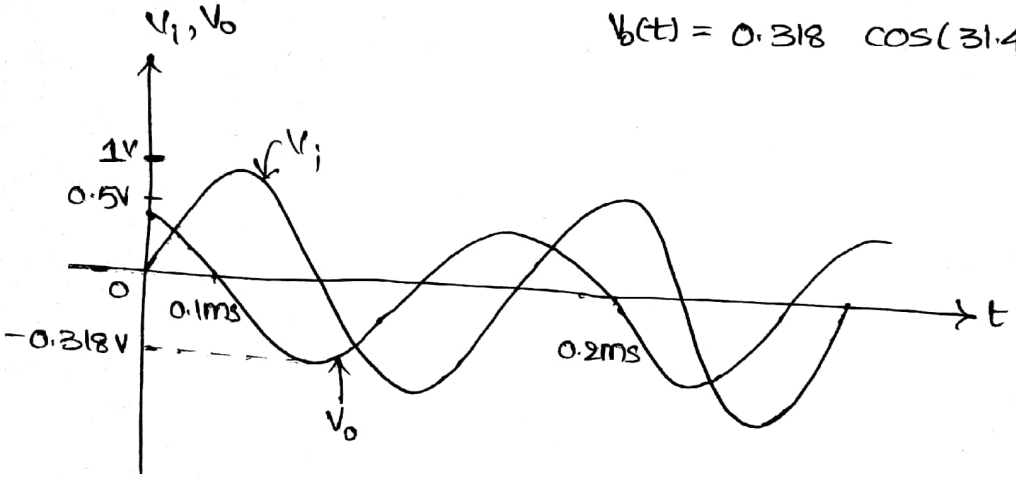
$\omega = 31.4\ KHz$

output of practical integrator, $V_o(t) = \frac{-1}{R_1 C_f} \int V_i(t)\, dt$

$$V_o(t) = \frac{-1}{(10K)(10n)} \int \sin(31.4K)t\, dt$$

$$V_o(t) = \frac{\cos(31.4K)t}{(31.4K)(0.1)}$$

$V_o(t) = 0.318 \cos(31.4K)t$



ii) Step input, $V_i = 1V$

consider $0 \le t \le 0.3$ ms

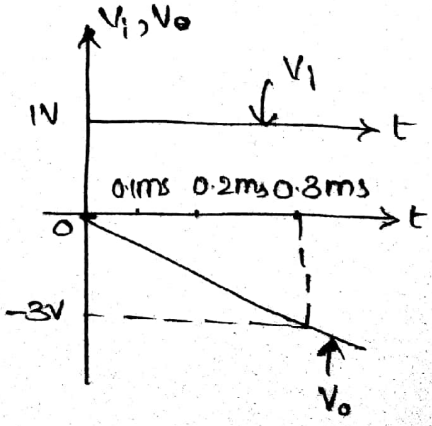
V_o at $t = 0.3$ ms is $V_o = \frac{-1}{R_1 C_f} \int_0^{0.3ms} 1 \cdot dt$

$$V_o = \frac{-1}{(10K)(10nf)} * (t)_0^{0.3ms}$$

$V_o = -10^4 \times 0.3 \times 10^{-3}$

$V_o = -3V$

The output voltage is rampfunction.,



(ii) Square wave input :, frequency = 5 KHz

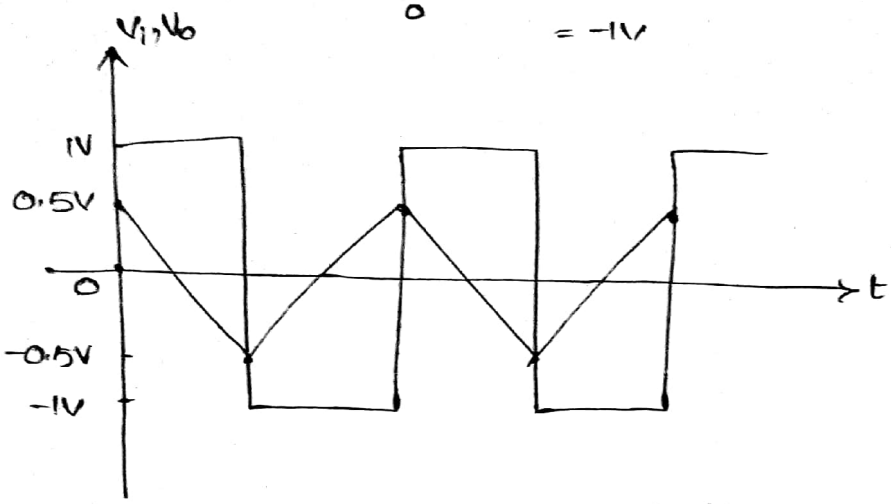
1V peak Square wave

$$V_i = \begin{cases} 1V & 0 \le t \le 0.1 \\ -1V & 0.1 \le t \le 0.2\,ms \end{cases}$$

The output of each of these half periods will be ramps as seen above for step inputs, thus the expected of waveform will be triangular wave.

$$V_0 = \frac{-1}{R_1 C_f} \int_0^{0.1ms} 1\,dt = -10^4 \times 0.1 \times 10^{-3}$$

$$= -1V$$



V-I convertor (voltage - current convertor):-

→ In voltage to current convertor, the output load current is proportion to the input voltage

$I_{OUT} \propto V_i$

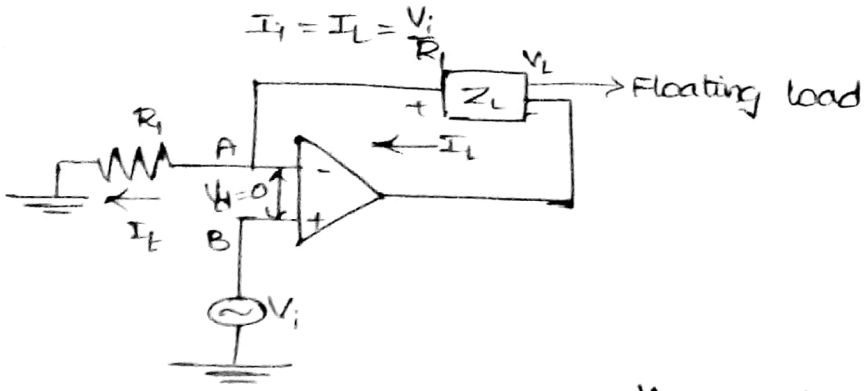
→ According to the connection of load, there are 2 types of V-I convertor

1. Voltage to current convertor with floating load.
2. Voltage to current convertor with grounded load.

→ It is also called as Transconductance amplifier.

1. Voltage to current convertor with floating load:

→ As input (voltage) current of op-amp is zero



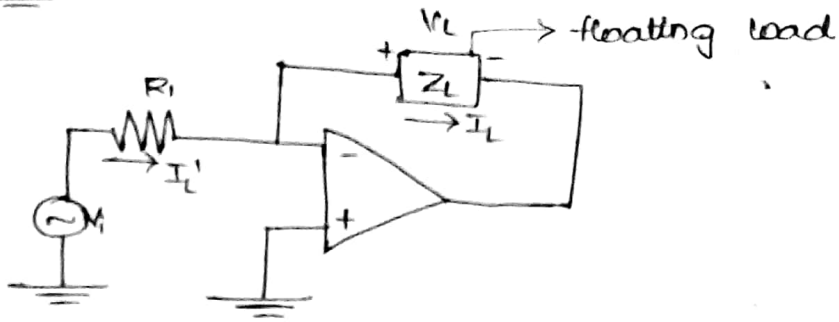
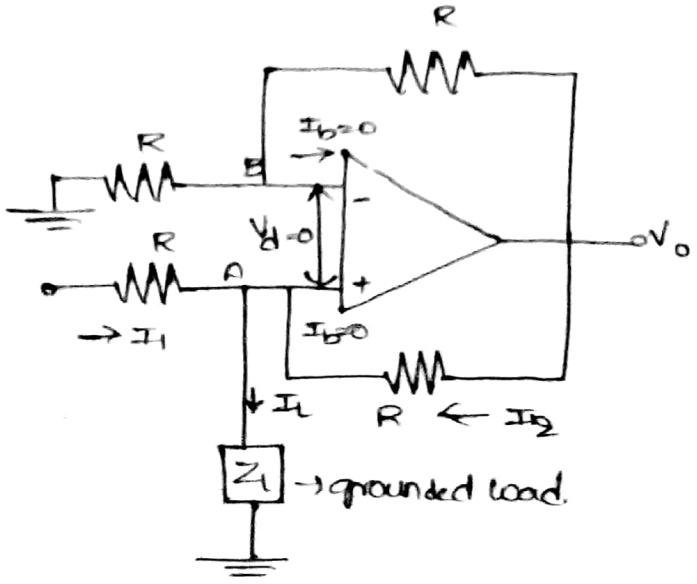


fig: floating load V-I convertors

$I_L \propto V_i$

→ Thus, the load current is proportional to the input voltage and circuit works as voltage to current converter.

2. Voltage to current Converter with grounded load:



It

→ As shown in above figure, one end of the load impedance Z_L is grounded. It is also known as "Howland Current Converter".

Circuit Analysis: $V_d = 0$

$V_A = V_B \quad (\because (V_B - V_A) = 0)$

Apply KCL at node A, $I_1 + I_2 = I_L$

$$I_L = \frac{V_i - V_A}{R} + \frac{V_o - V_A}{R}$$

$$I_L R = V_i + V_o - 2V_A$$

$$V_A = \frac{V_i + V_o - I_L R}{2} \rightarrow (1)$$

For inverting amplifier, the $V_o = \left(1 + \frac{R_f}{R_1}\right) V_A$

$$= \left(1 + \frac{R}{R}\right) V_A = 2V_A$$

$$V_o = 2V_A \rightarrow (2)$$

Substitute the value of V_A in eq. (1),

$$\frac{V_o}{R} = \frac{V_i}{2} = \frac{I_L \cdot R}{2} + \frac{V_o}{2}$$

$$\frac{I_L R}{2} = \frac{V_i}{2}$$

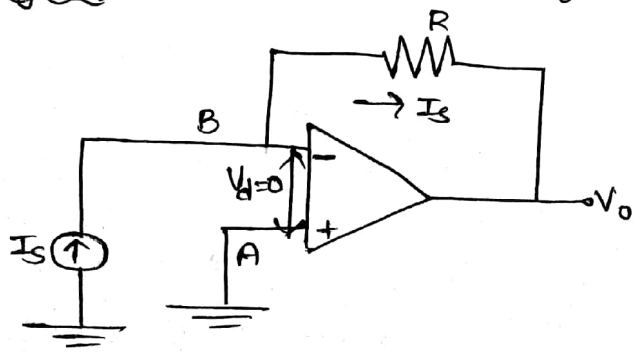
$$I_L = \frac{V_i}{R}$$

Since R is constant, $\boxed{I_L \propto V_i}$

Current (I) to Voltage (V) converter:-

$V_o \propto I_i$

Circuit diagram:-



→ In this, the o/p voltage is proportional to its input current.

→ It accepts an i/p (voltage) current I_s and produces an output voltage, V_o such that $V_o = A I_s$.

where A is the gain of the circuit.

→ Since A is measured in ohms Because of this, I-V converters are also called transresistance amplifier.

Circuit Analysis:- $V_d = 0$

$V_B - V_A = 0$

$V_A = V_B$ Since $V_A = 0 \Rightarrow V_B = 0$

Now, $\frac{V_B - V_o}{R_f} = I_s \Rightarrow I_s = \frac{-V_o}{R_f}$

$V_o = -I_s R_f$

As R_f is constant

$\boxed{V_o \propto I_s}$

→ The output voltage is proportional to the input current & the circuit works as a current to voltage converter.

→ This circuit also referred as current controlled voltage source.

→ If the resistance in the circuit is replaced by the impedance, Z the circuit is called trans-impedance amplifier.

(Basic) logarithmic Amplifier:-

The voltage (output) of logarithmic amplifier is

$V_o \propto \log(V_i)$

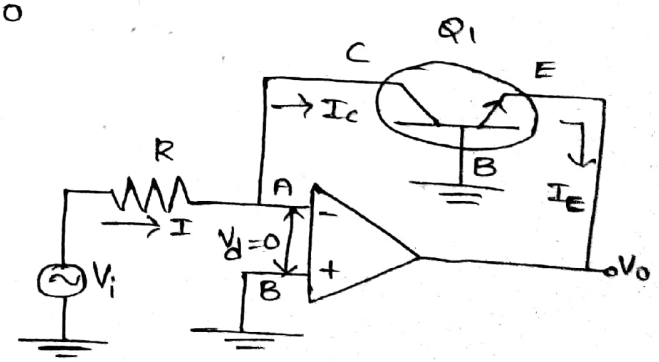
(Or) $V_o \propto \ln_e(V_i)$

Basic logarithmic circuit:-

The difference voltage, $V_d = 0$

$V_A = 0$

Since transistor the base terminal is grounded implies I_E and I_C are equal.



The diode current equation is $I_C = I_s \left(e^{\frac{qV_{BE}}{KT}} - 1\right) \rightarrow (1)$

where I_s represents reverse saturation current and its value is 10^{-13} A.

$$V_o = \frac{-(1.38\times10^{-23}\times300)}{1.602\times10^{-19}} \ln_e\left(\frac{V_i}{10^{-13}\times10^{3}\times10}\right)$$

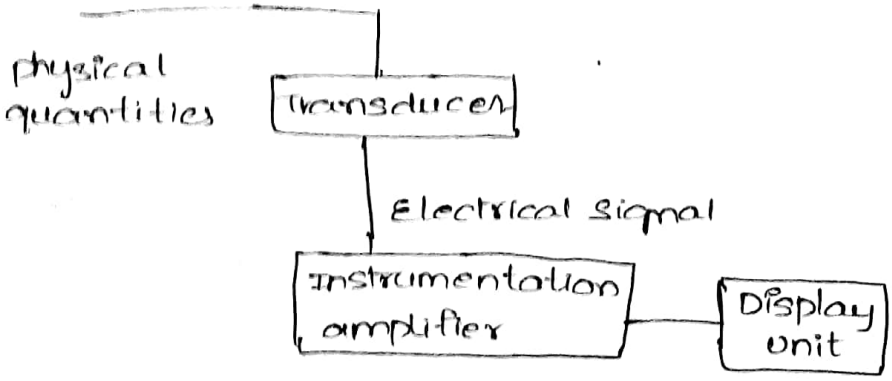
$$V_o = -0.0258 \ln_e\left(\frac{V_i}{10^{-19}}\right)$$

when $V_i = 5mV$ then $V_o = -0.397\ V$

when $V_i = 50mV$ then $V_o = -0.45V$

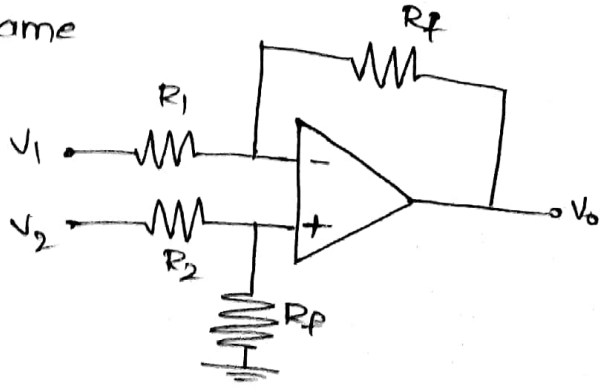
Instrumentation Amplifier:

The Instrumentation amplifier is mostly used in industrial applications in order to measure the change in physical quantities (Temperature, humidity, intensity...)



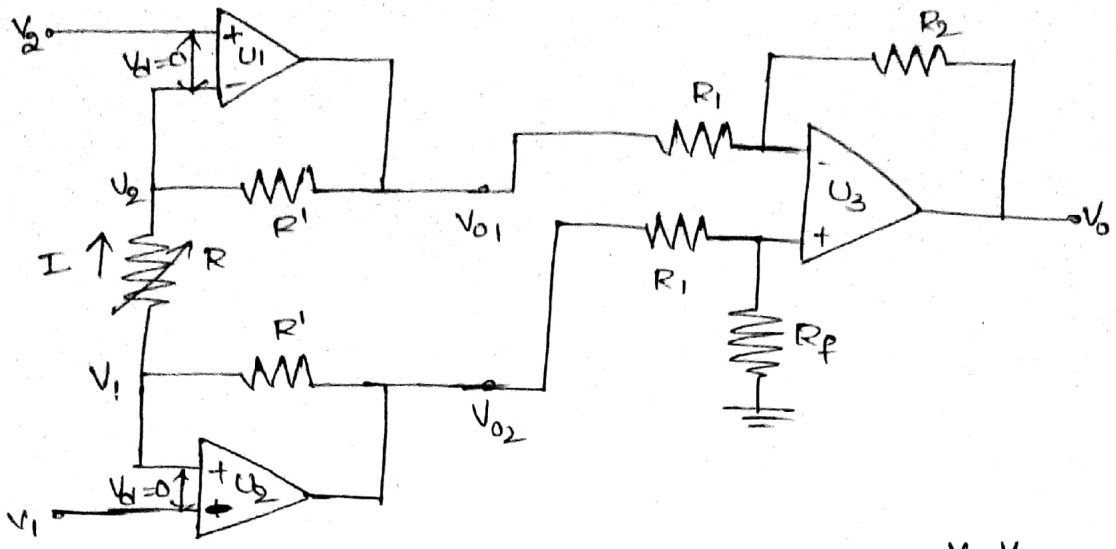
The basic circuit of instrumentation amplifier is a difference amplifier.

Derive the output voltage same as difference amplifier output voltage.



-At V_1 terminal, the I/p impedance is $R_1 + R_f$ at V_2 terminal, the I/p impedance is $R_1 + R_f$.

Since the instrumentation amplifier is used in middle of part. It has to provide high input impedance and low output impedance with the use of difference amplifier it doesnot provide high input impedance. In order to provide high input impedance, a high impedance buffers are used before V_1 and V_2.



The current flows through the resistor R is $I = \frac{V_1 - V_2}{R}$

If V_1 and V_2 are equal there is no current flow through the potentiometer R.

If V_1 and V_2 are not equal.,

$$-V_1 - IR' + V_{02} = 0$$

$$V_{02} = V_1 + IR'$$

The o/p voltage of high impedance buffer(U_1) is

$$V_{01} = V_2 - IR'$$

The o/p voltage of difference amplifier is

$$V_o = \frac{R_2}{R_1}(V_{02} - V_{01})$$

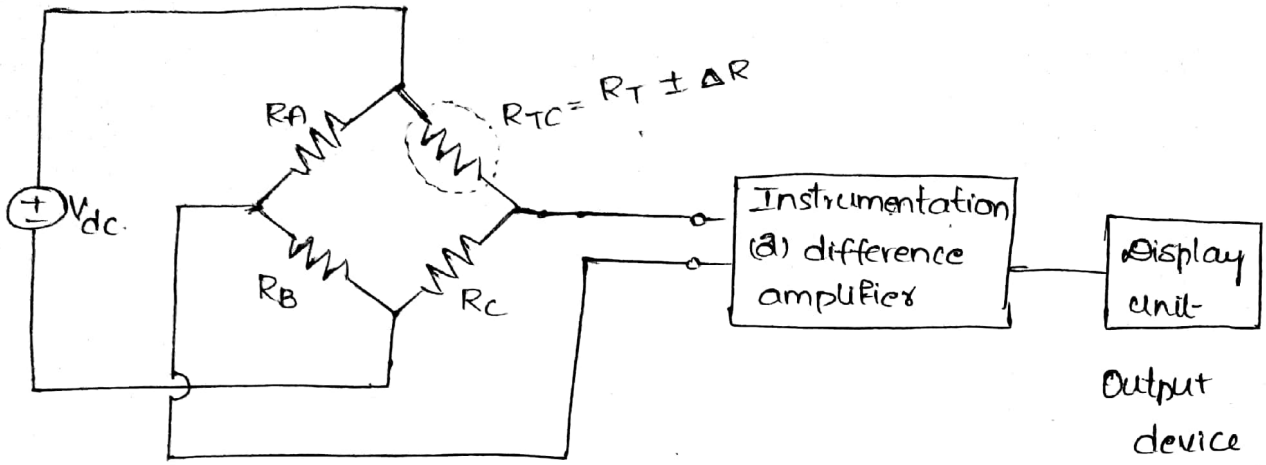
$$= \frac{R_2}{R_1}(V_1 + IR' - V_2 + IR')$$

$$= \frac{R_2}{R_1}((V_1 - V_2) + 2IR')$$

$$= \frac{R_2}{R_1}\left(\frac{2(V_1 - V_2)}{R}R' + (V_1 - V_2)\right)$$

$$\boxed{V_o = (V_1 - V_2)\left(\frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)\right)}$$

The instrumentation amplifier using transducer bridge (or) Wein stone bridge.



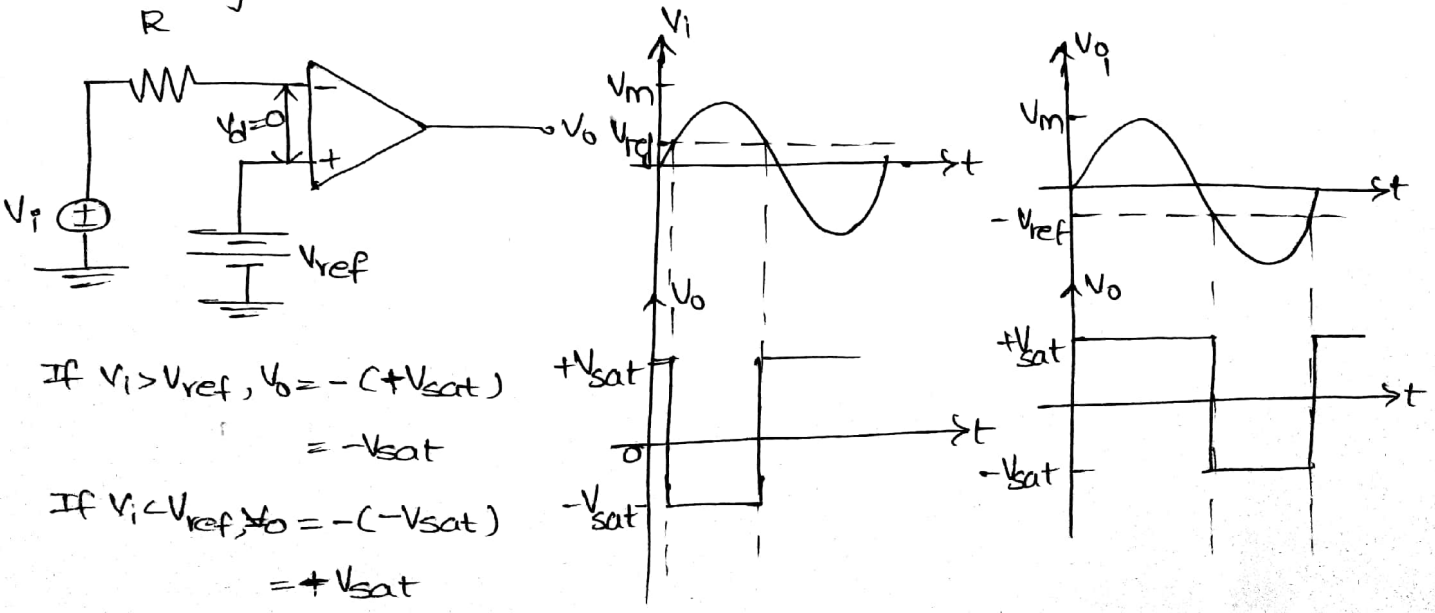
Transducer / Wein stone bridge

The transducer bridge uses a resistive element at one arm that depends on physical quantity. The Bridge is intially in balanced mode if there is a change in physical quantity then the bridge becomes unbalanced. This voltage is given as i/p to 3-op-amp instrumentational amplified which is used to drive the display unit.

Comparators:-

The comparator using op-amp operates in open loop mode. For non-linear applications the comparator is mainly used

i) Inverting comparator:- when the input signal is given to inverting terminal of op-amp and a fixed dc voltage is given to non-inverting terminal then it is called as Inverting comparator.



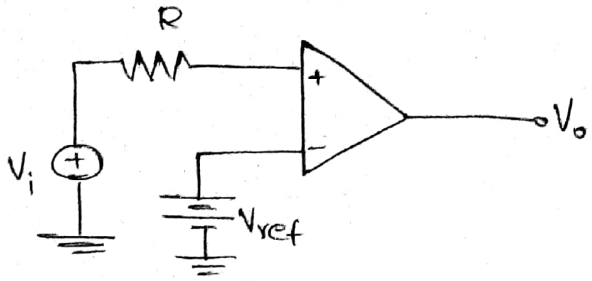
If $V_i > V_{ref}$, $V_o = -(+V_{sat})$

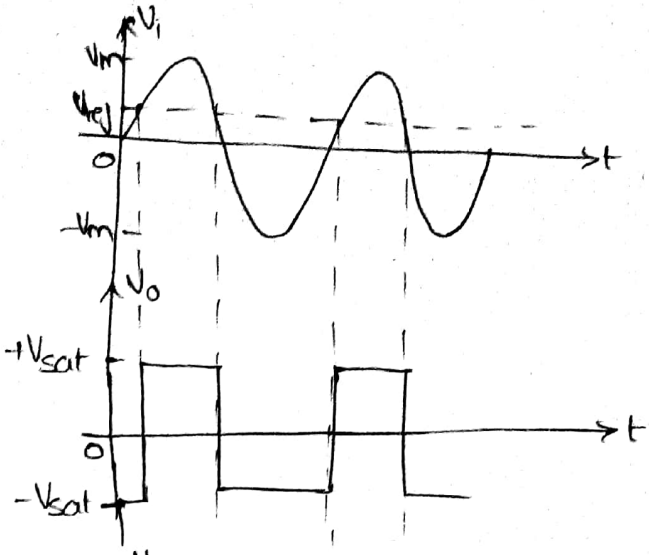
$= -V_{sat}$

If $V_i < V_{ref}$, $V_o = -(-V_{sat})$

$= +V_{sat}$

ii) Non - Inverting terminal, when the i/p signal is given to non-inverting terminal of op-amp & the reference voltage is given to inverting terminal then it is called as Non-inverting comparator.



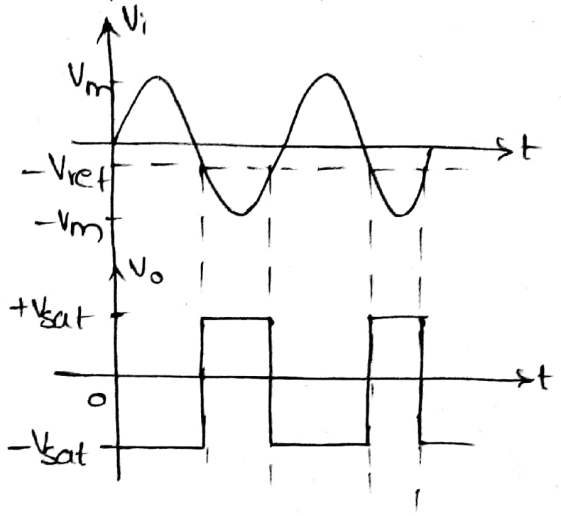


If $V_i > V_{ref}$, $V_o = +(+V_{sat})$

$V_o = +V_{sat}$

If $V_i < V_{ref}$, $V_o = +(-V_{sat})$

$= -V_{sat}$



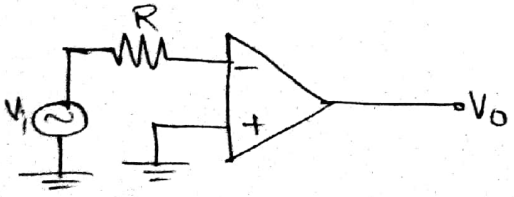
Applications of comparator:-

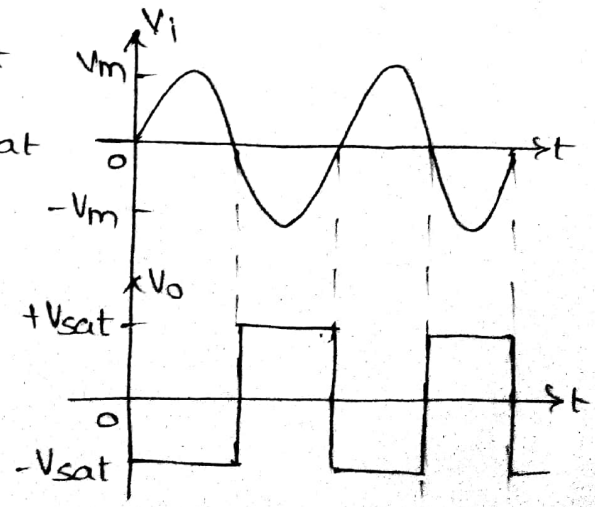
1. Zero Crossing detector., when the reference voltage is 0V then the circuit is said to be in zero crossing detector mode.

a) Inverting type Zero Crossing detector:-

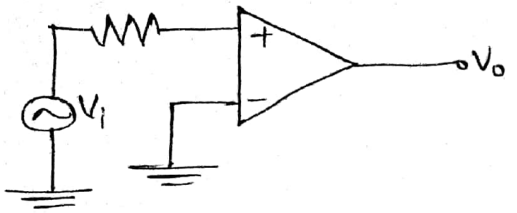
when $V_i > 0$, $V_o = -(+V_{sat}) = -V_{sat}$

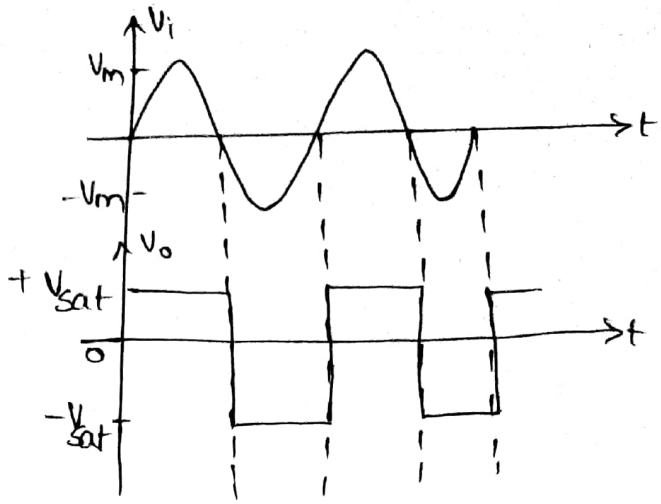
when $V_i < 0$, $V_o = -(-V_{sat}) = +V_{sat}$





b) Non-Inverting type zero crossing detector:



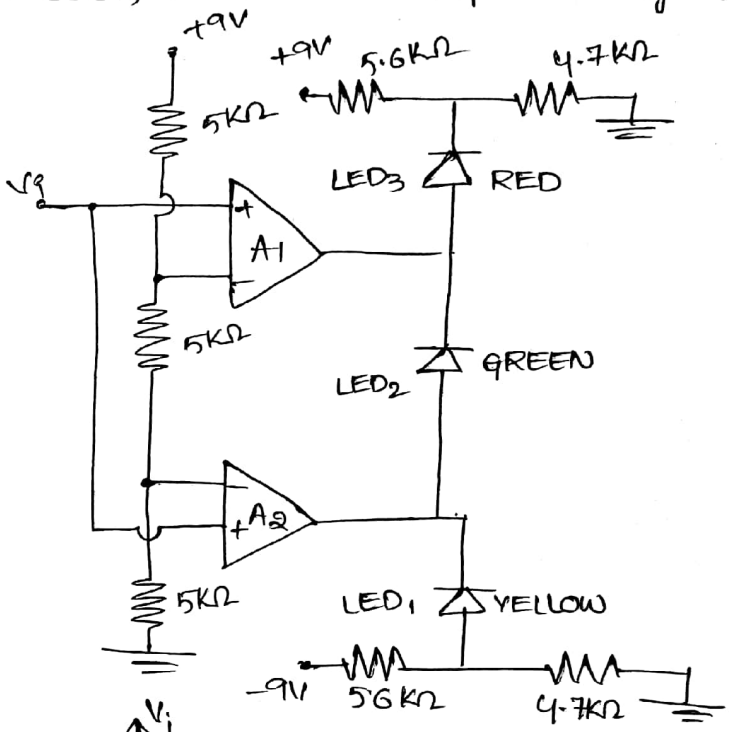


When $V_i > 0$, $V_o = +(+V_{sat}) = +V_{sat}$

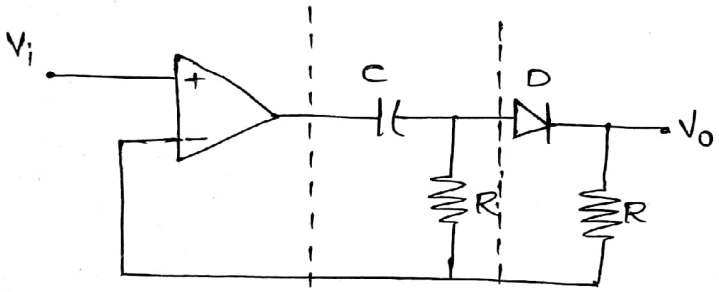
When $V_i < 0$, $V_o = +(-V_{sat}) = -V_{sat}$

2) Window detector: By using the detector, the unknown input voltage range can be found.

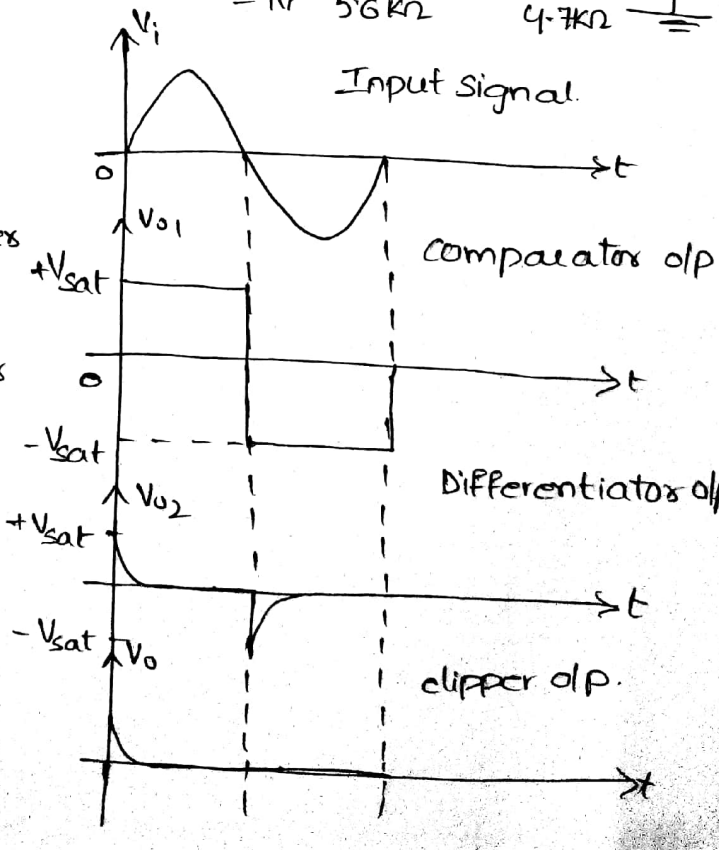
I/p voltage	Yellow	Green	Red
$V_i < 3V$	ON	OFF	OFF
$3V < V_i < 6V$	OFF	ON	OFF
$V_i > 6V$	OFF	OFF	ON



3) Time markers generators:



It is used to generate trigger signals and mainly used in one shot (or) monostable multivibrator.

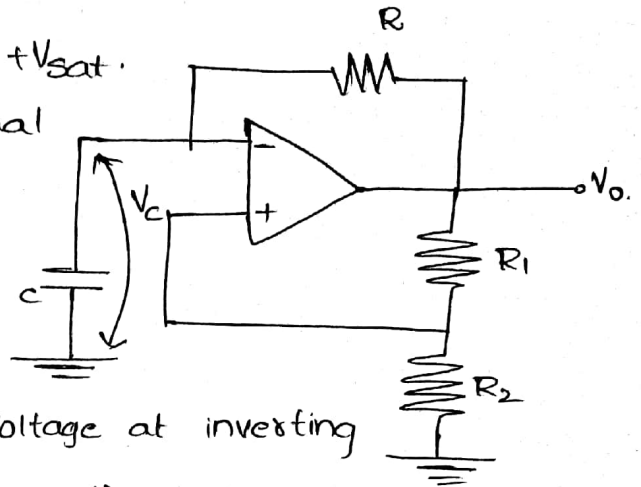


4. phase detector :- It is same as time marker generator but at the input a phase detector is used

Multivibrators :-

Astable Multivibrator :-

It is also called as square wave generator (or) free running oscillator (or) Relaxation oscillator. In this 2 quasi stable states are present and it doesn't require any triggering to change its states.

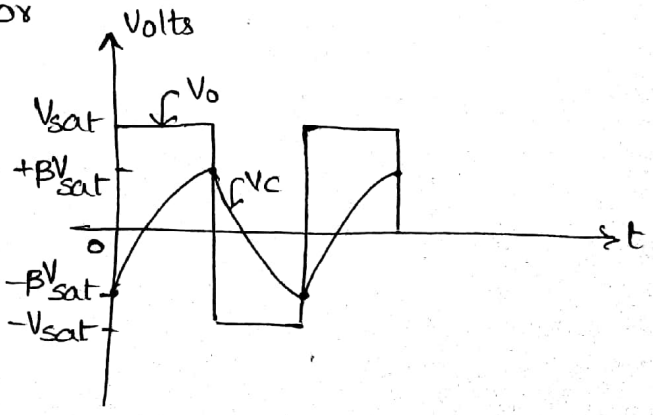


consider the output is at $+V_{sat}$. The voltage at +ve input terminal is $+\beta V_{sat}$ (β is $\frac{R_2}{R_1+R_2}$) at this instant of time, the capacitor starts charging towards to $+V_{sat}$ through the resistor R. when the voltage at inverting terminal becomes just greater than the reference voltage ($+\beta V_{sat}$) the output is suddenly drops to $-V_{sat}$. At this point, the capacitor starts discharging through resistor R of value $-\beta V_{sat}$. when the voltage at the inverting terminal becomes less than $-\beta V_{sat}$. The output is driven to +ve V_{sat} & the cycle repeats.

Frequency of Oscillations for Square wave generator :-

The voltage across the capacitor as a function of time is given as

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$



from the waveforms.,

$$V_f = +V_{sat} \qquad V_i = \beta V_{sat}$$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

$$= V_{sat}\left[\left[1 - (1+\beta)\right] e^{-t/RC}\right]$$

$$t = T_1, \quad V_c(t) = \beta V_{sat}$$

$$\beta V_{sat} = V_{sat}\left[1 - (1+\beta)\, e^{-T_1/RC}\right]$$

$$(1+\beta)e^{-T_1/RC} = 1-\beta$$

$$e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$$

$$-T_1/RC = \ln\left(\frac{1-\beta}{1+\beta}\right)$$

$$T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$T_1 = T_2$$

$$\Rightarrow T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

Assume $\beta = 0.5$, $R_1 = R_2$

$$T = 2RC \ln\left(\frac{3/2}{1/2}\right)$$

$$T = 2RC \ln(3)$$

$$T = 2.19\,RC$$

$$T \simeq 2.2\,RC$$

$$f = \frac{1}{T} = \frac{1}{2.2RC}$$

The peak to peak amplitude of square wave generator is

$$V_{o(p-p)} = 2V_{sat}$$

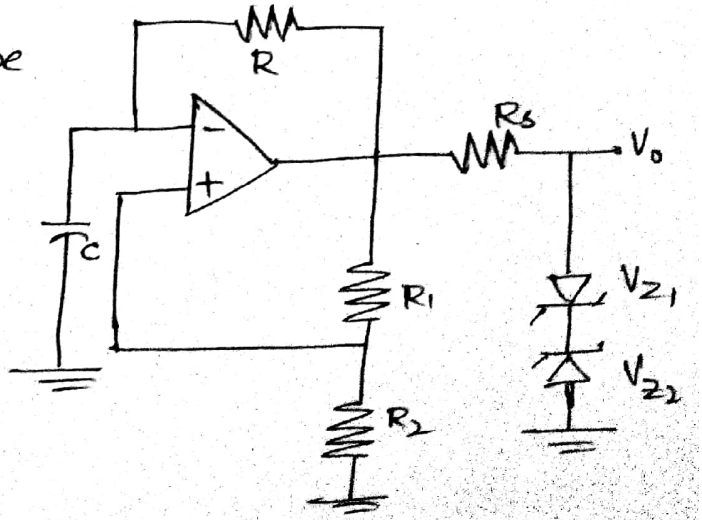
The amplitude can be varied, the power supply voltage. The peak amplitude can also be varied by making the power supply constant and the use of zener diodes connected back to back at the output. The output voltage is the summation of saturation voltage and zener break down voltage.

Symmetrical square wave can be generated if $V_{Z1} = V_{Z2}$

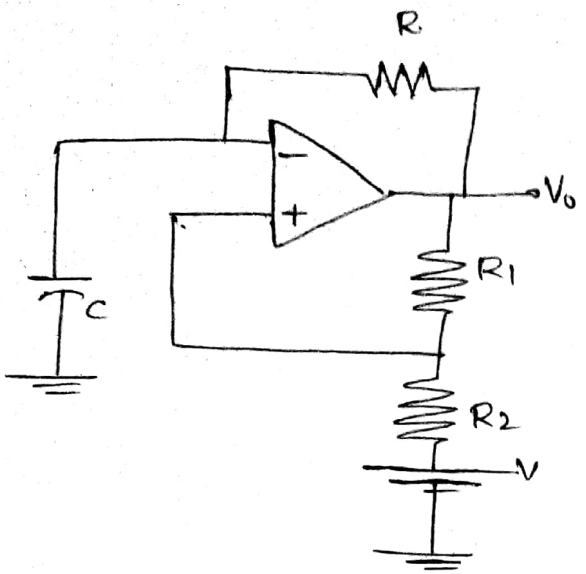
$\Rightarrow T_1 = T_2$

Asymmetrical square wave can be generated if $V_{Z1} \neq V_{Z2}$

$\Rightarrow T_1 \neq T_2$



An alternative method for generating asymmetrical square wave by using voltage to frequency converter



The capacitor charging and discharging voltages are given as:

charging voltage is $+\beta V_{sat} + V$.

discharging voltage is $-\beta V_{sat} + V$

The ON time, $T_{ON} / T_1 = RC \ln\left(\frac{1+\beta(V_{o2}/V_{o1})}{1-\beta}\right)$

The OFF time, $T_{OFF} / T_2 = RC \ln\left(\frac{1+\beta(V_{o1}/V_{o2})}{1-\beta}\right)$

Problems:-

1. Design a free running oscillator with T_{ON} of value 0.1 ms and T_{off} is 0.2 ms.

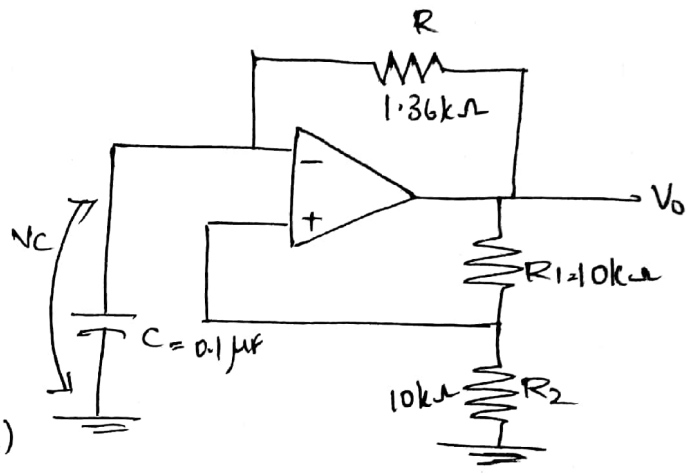
Sol:- Given $T_{ON} = 0.1 ms$

$T_{OFF} = 0.2 ms$

$T = T_{ON} + T_{off}$

$T = 0.1 + 0.2 = 0.3 ms$

Assume $\beta = 0.5$ $(R_1 = R_2)$



let $R_1 = 10K\Omega$. $\Rightarrow R_2 = 10K\Omega$

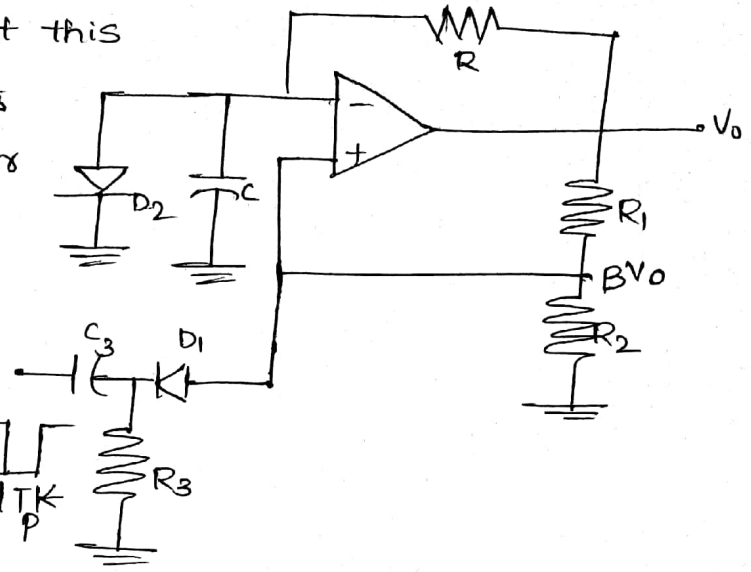
$T = 2.2RC \Rightarrow C \leq 1\mu F \Rightarrow C = 0.1\mu F$

$0.3 \times 10^{-3} = 2.2 \times R \times 0.1 \times 10^{-6}$

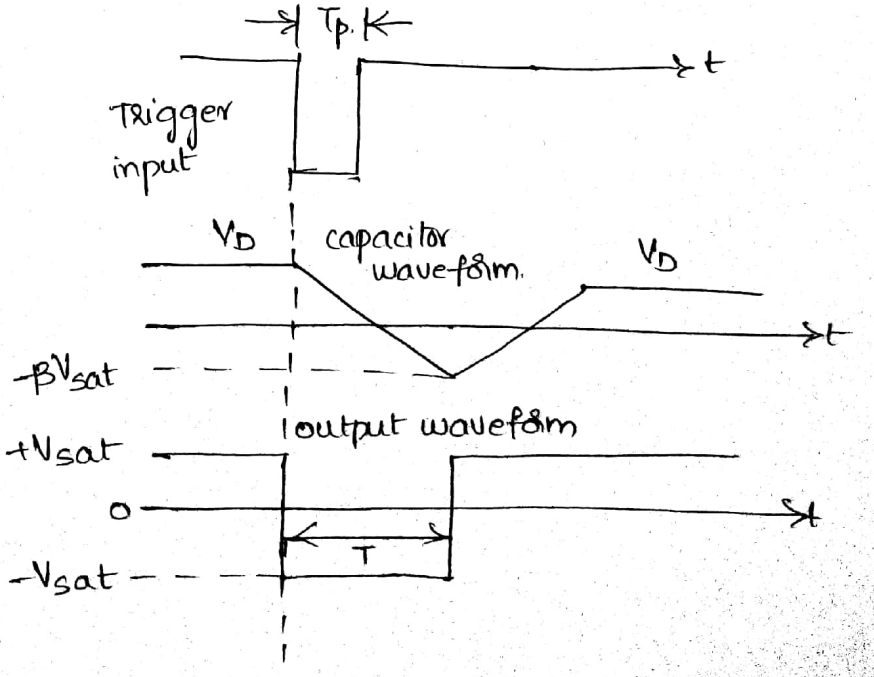
$R = 1.36\ K\Omega$

Monostable Multivibrator:-

It is also called as one shot multivibrator delay circuit (or) gating circuit It needs one trigger pulse to change its state. The monostable multivibrator is used in sampling gates.



Consider V_o is $+V_{sat}$. At this instant the capacitor starts charging when the capacitor voltage reaches to 0.7V. The diode D_2 will go ON implies V_c is clamped to 0.7V. A negative trigger pulse is applied at the non-inverting terminal of op-amp whose voltage is $\beta V_{sat} - V_1$ which is always 0.7V. Hence the output of op-amp will switch from $+V_{sat}$ to $-V_{sat}$. Due to this the diode D_2 will be in reverse bias & the capacitor starts discharging to $-V_{sat}$ through the resistor R. If the voltage at non-inverting terminal is high compared to inverting terminal. The output of op-amp again switches from $-V_{sat}$ to $+V_{sat}$ and the cycle repeats.



Expression for pulse width:-

The voltage across capacitor is $V_c(t) = V_f + (V_i - V_f)e^{-t/RC}$

from the waveform, $V_f = -V_{sat}$ $V_i = V_D$

$$V_c(t) = -V_{sat} + (V_D + V_{sat})e^{-t/RC}$$

At $t = T$, $V_c(t) = -\beta V_{sat}$

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

$$-\beta V_{sat} = V_{sat}\left[-1 + \left(\frac{V_D}{V_{sat}} + 1\right)e^{-T/RC}\right]$$

$$-\beta = -1 + \left(\frac{V_D}{V_{sat}} + 1\right)e^{-T/RC}$$

$$1 - \beta = \left(1 + \frac{V_D}{V_{sat}}\right)e^{-T/RC}$$

$$e^{T/RC} = \frac{(1 + (V_D/V_{sat}))}{1-\beta}$$

$$\frac{T}{RC} = \ln\left[\frac{1 + (V_D/V_{sat})}{1-\beta}\right]$$

$$T = RC \ln\left[\frac{1 + (V_D/V_{sat})}{1-\beta}\right]$$

$V_D = 0.7V$; $V_{sat} = 15V$

$$\frac{V_D}{V_{sat}} = \frac{0.7}{15} = 0.046 < 1.$$

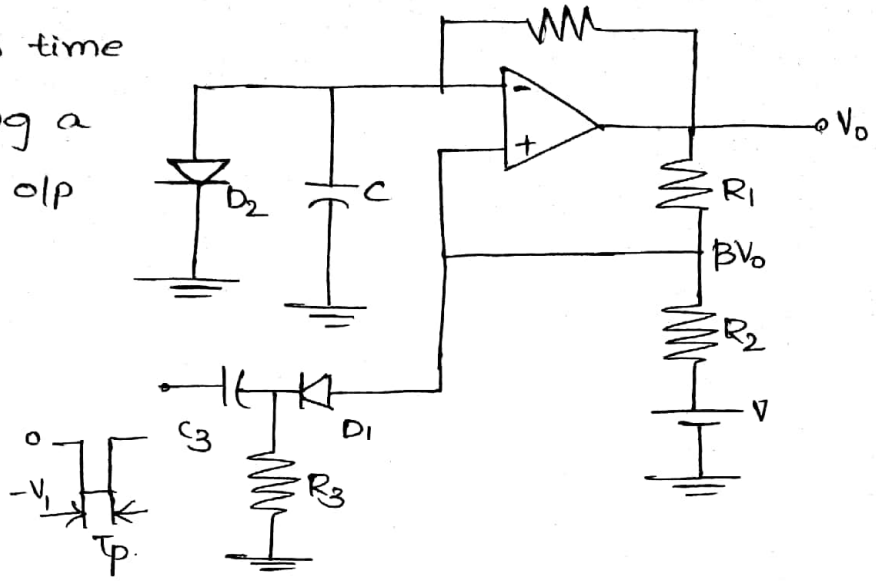
Eliminate (V_D/V_{sat}).,

$$T = RC \ln\left(\frac{1}{1-\beta}\right)$$

when $\beta = 0.5$., $T = RC \ln(2)$

$$\boxed{T = 0.693RC}$$

The monostable multivibrator can be used as voltage to time convertor by adding a dc voltage at the o/p side.



problem:-

1. Design a monostable multivibrator whose pulse width is 650 μsec, the saturation voltage is 9V, which is triggered by an input voltage & input pulse of value 3V. & the time period 50 μsec.

Sol:- Given $-V_1 = 3V \Rightarrow V_1 = -3V$

$T_p = 50\,\mu sec$

$+V_{sat} = \pm 9V$

$T = 650\,\mu sec$

$T = RC \ln\left(\frac{1}{1-\beta}\right)$

Assume $\beta = 0.5 \Rightarrow R_1 = R_2 = 10\,K\Omega$

$T = 0.693\,RC$

$650\,\mu s = T$

let $0.1\,\mu F = C$

$650\,\mu = 0.693(0.1\,\mu)R$

$$\boxed{R = 9.37\ K\Omega}$$

$R_3 C_3 < T_p$

let $\boxed{C_3 = 0.1\,\mu F}$

$R_3 < \frac{50\,\mu}{0.1\,\mu}$

$$\boxed{R_3 < 500\,\Omega}$$

$$V_o = \frac{-(1.38\times10^{-23}\times300)}{1.602\times10^{-19}} \ln_e\left(\frac{V_i}{10^{-13}\times10^{3}\times10}\right)$$

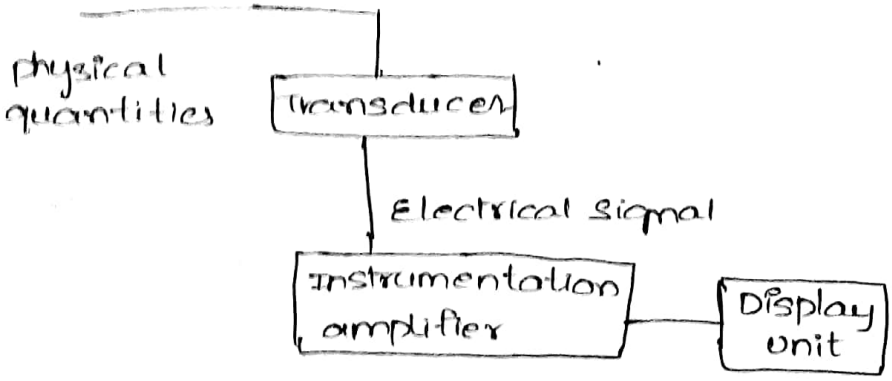
$$V_o = -0.0258 \ln_e\left(\frac{V_i}{10^{-19}}\right)$$

when $V_i = 5mV$ then $V_o = -0.397\ V$

when $V_i = 50mV$ then $V_o = -0.45V$

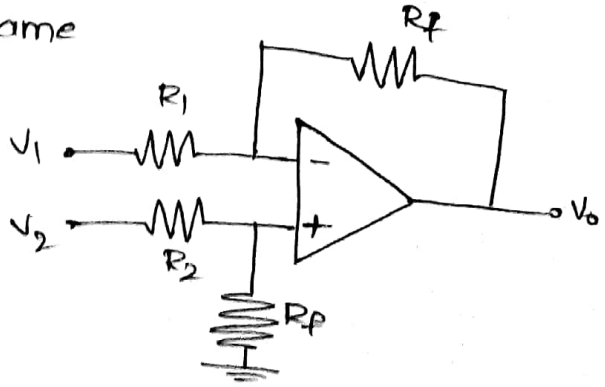
Instrumentation Amplifier:

The Instrumentation amplifier is mostly used in industrial applications in order to measure the change in physical quantities (Temperature, humidity, intensity...)



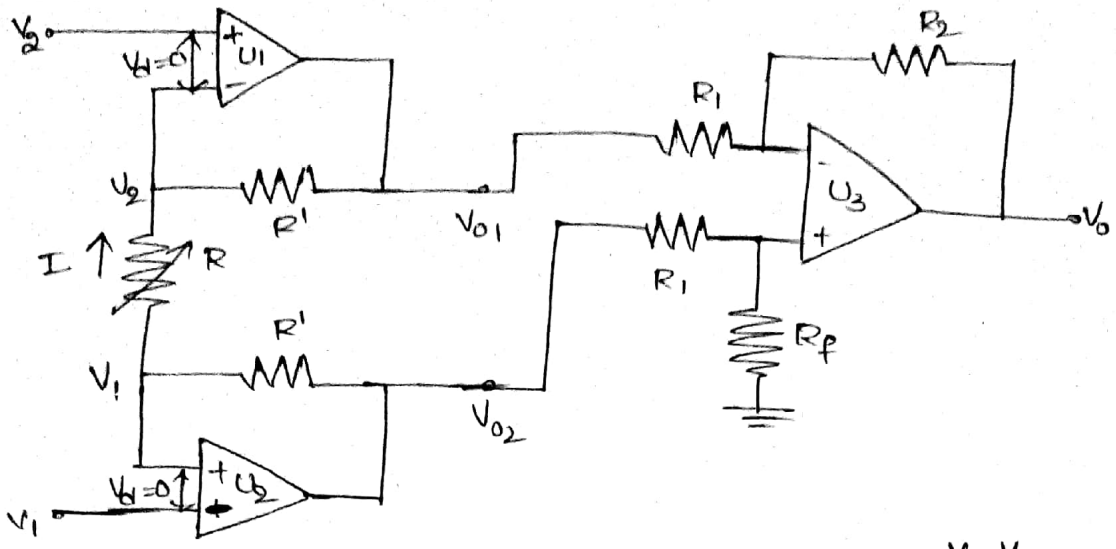
The basic circuit of instrumentation amplifier is a difference amplifier.

Derive the output voltage same as difference amplifier output voltage.



-At V_1 terminal, the I/p impedance is $R_1 + R_f$ at V_2 terminal, the I/p impedance is $R_1 + R_f$.

Since the instrumentation amplifier is used in middle of part. It has to provide high input impedance and low output impedance with the use of difference amplifier it doesnot provide high input impedance. In order to provide high input impedance, a high impedance buffers are used before V_1 and V_2.



The current flows through the resistor R is $I = \frac{V_1 - V_2}{R}$

If V_1 and V_2 are equal there is no current flow through the potentiometer R.

If V_1 and V_2 are not equal.,

$$-V_1 - IR' + V_{02} = 0$$

$$V_{02} = V_1 + IR'$$

The o/p voltage of high impedance buffer(U_1) is

$$V_{01} = V_2 - IR'$$

The o/p voltage of difference amplifier is

$$V_o = \frac{R_2}{R_1}(V_{02} - V_{01})$$

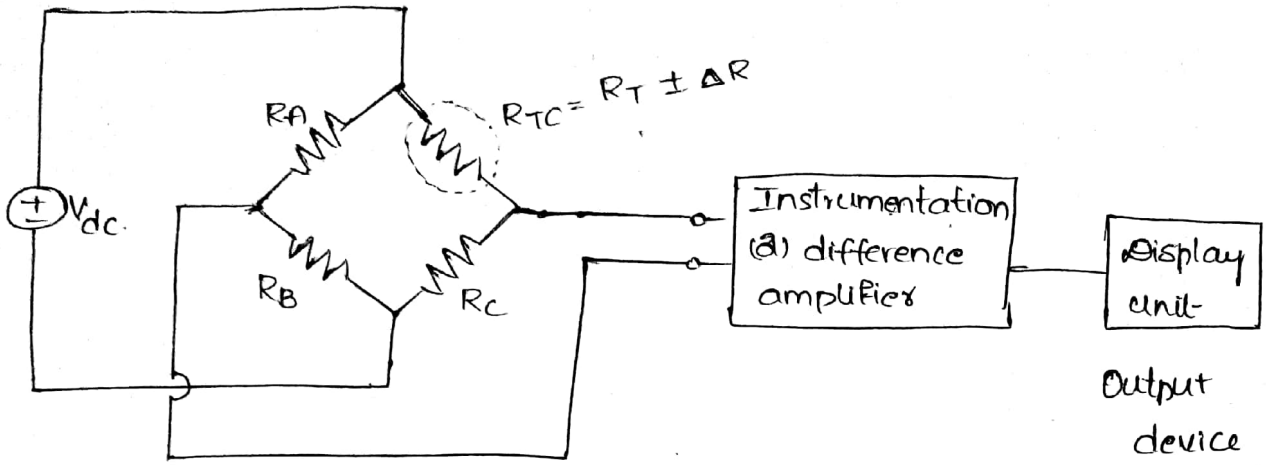
$$= \frac{R_2}{R_1}(V_1 + IR' - V_2 + IR')$$

$$= \frac{R_2}{R_1}((V_1 - V_2) + 2IR')$$

$$= \frac{R_2}{R_1}\left(\frac{2(V_1 - V_2)}{R}R' + (V_1 - V_2)\right)$$

$$\boxed{V_o = (V_1 - V_2)\left(\frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)\right)}$$

The instrumentation amplifier using transducer bridge (or) Wein stone bridge.



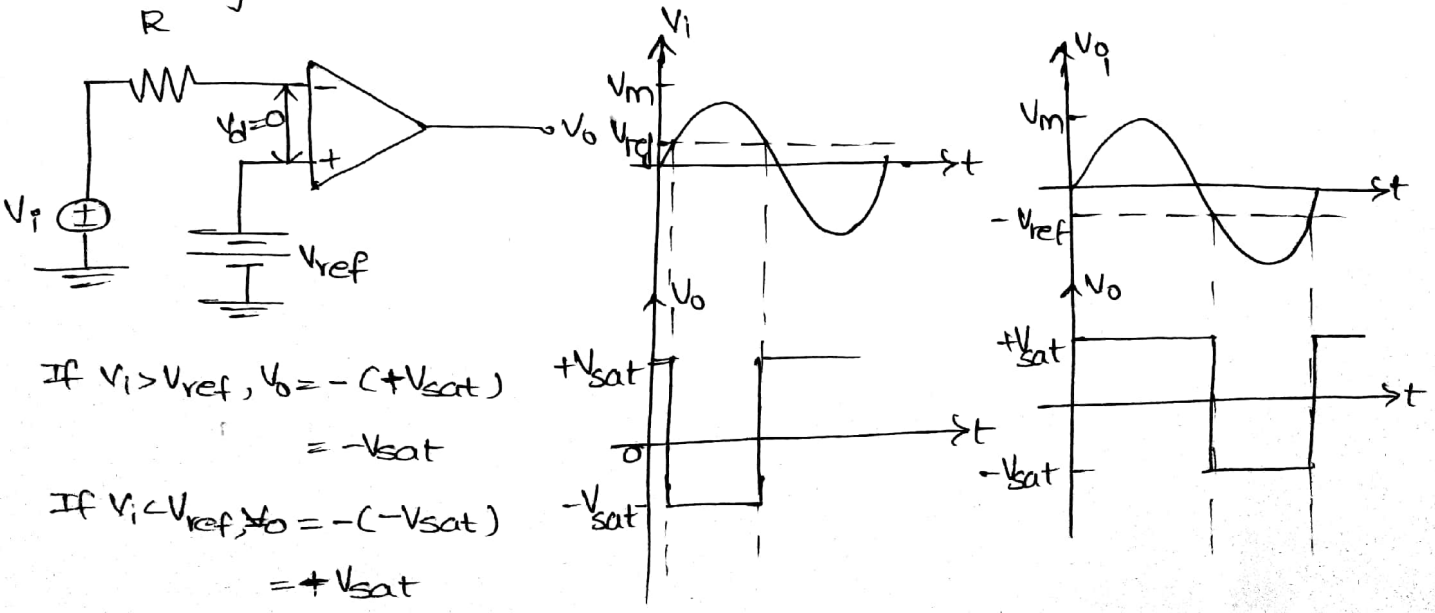
Transducer / Wein stone bridge

The transducer bridge uses a resistive element at one arm that depends on physical quantity. The Bridge is intially in balanced mode if there is a change in physical quantity then the bridge becomes unbalanced. This voltage is given as i/p to 3-op-amp instrumentational amplified which is used to drive the display unit.

Comparators:-

The comparator using op-amp operates in open loop mode. For non-linear applications the comparator is mainly used

i) Inverting comparator:- when the input signal is given to inverting terminal of op-amp and a fixed dc voltage is given to non-inverting terminal then it is called as Inverting comparator.



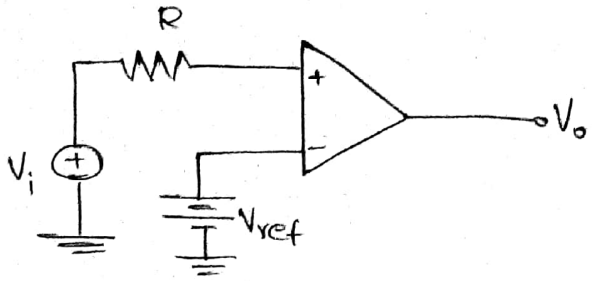
If $V_i > V_{ref}$, $V_o = -(+V_{sat})$

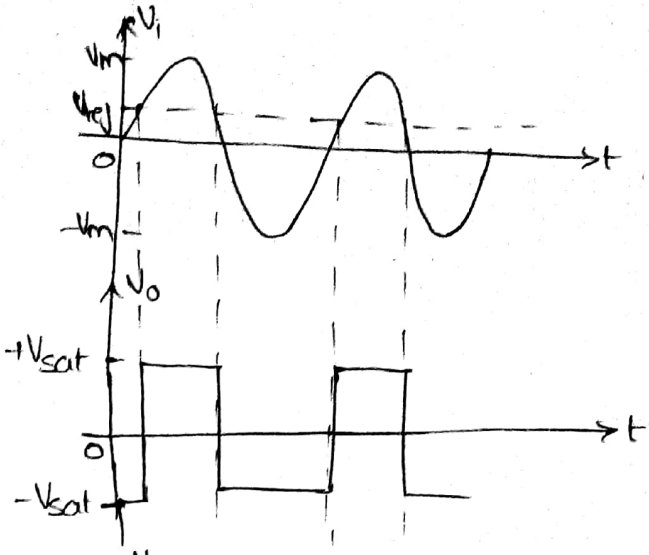
$= -V_{sat}$

If $V_i < V_{ref}$, $V_o = -(-V_{sat})$

$= +V_{sat}$

ii) Non - Inverting terminal, when the i/p signal is given to non-inverting terminal of op-amp & the reference voltage is given to inverting terminal then it is called as Non-inverting comparator.



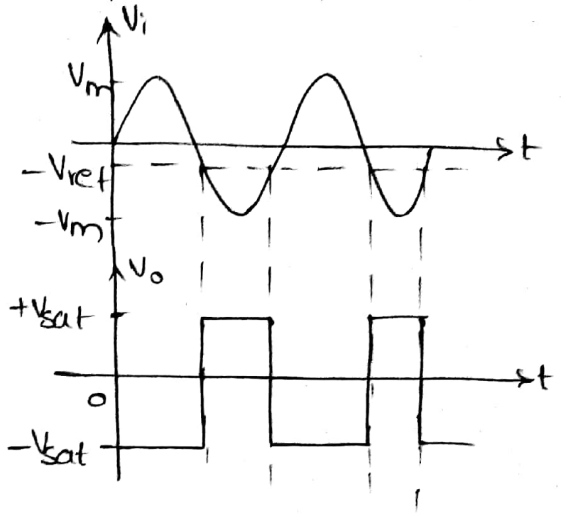


If $V_i > V_{ref}$, $V_o = +(+V_{sat})$

$V_o = +V_{sat}$

If $V_i < V_{ref}$, $V_o = +(-V_{sat})$

$= -V_{sat}$



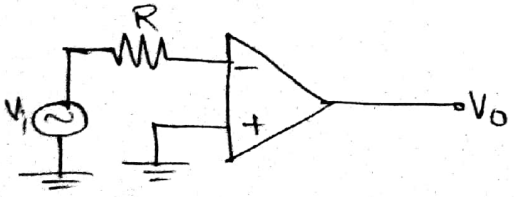
Applications of comparator:-

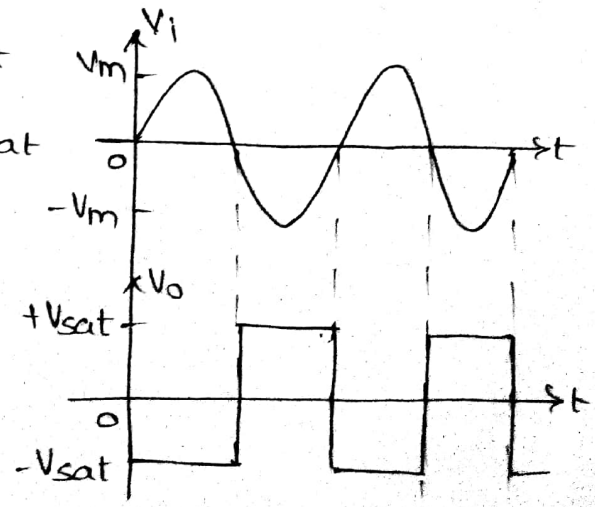
1. Zero Crossing detector., when the reference voltage is 0V then the circuit is said to be in zero crossing detector mode.

a) Inverting type Zero Crossing detector:-

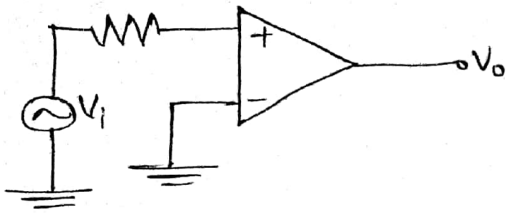
when $V_i > 0$, $V_o = -(+V_{sat}) = -V_{sat}$

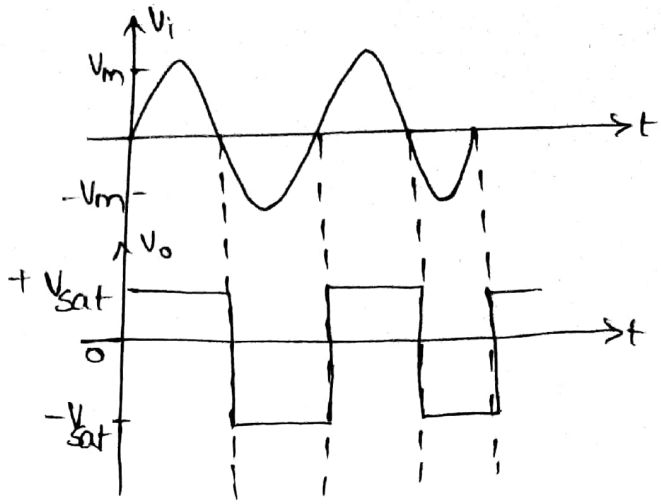
when $V_i < 0$, $V_o = -(-V_{sat}) = +V_{sat}$





b) Non-Inverting type zero crossing detector:



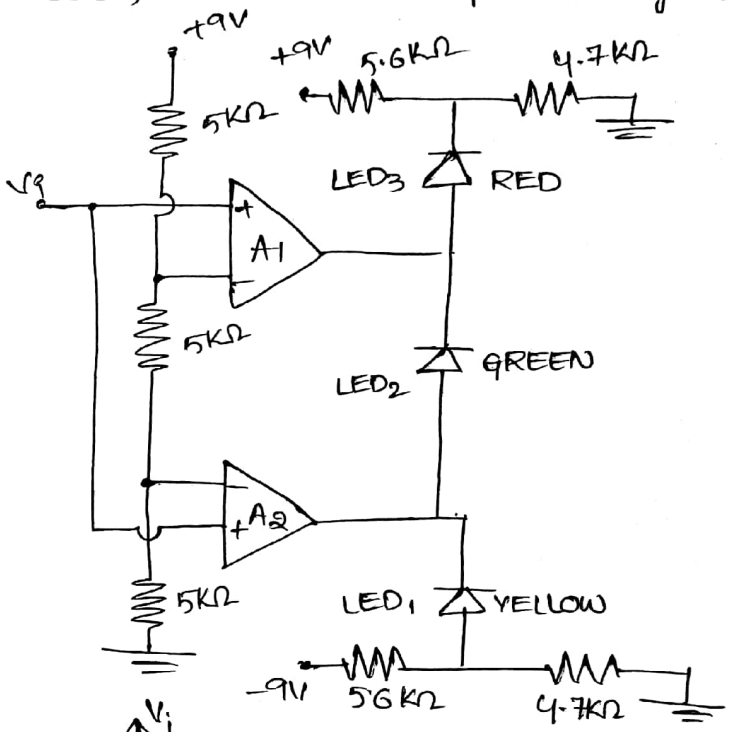


When $V_i > 0$, $V_o = +(+V_{sat}) = +V_{sat}$

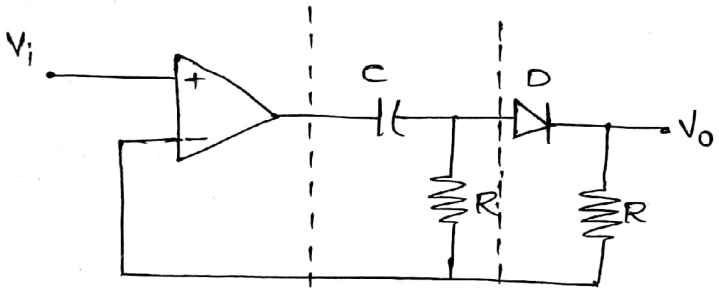
When $V_i < 0$, $V_o = +(-V_{sat}) = -V_{sat}$

2) Window detector: By using the detector, the unknown input voltage range can be found.

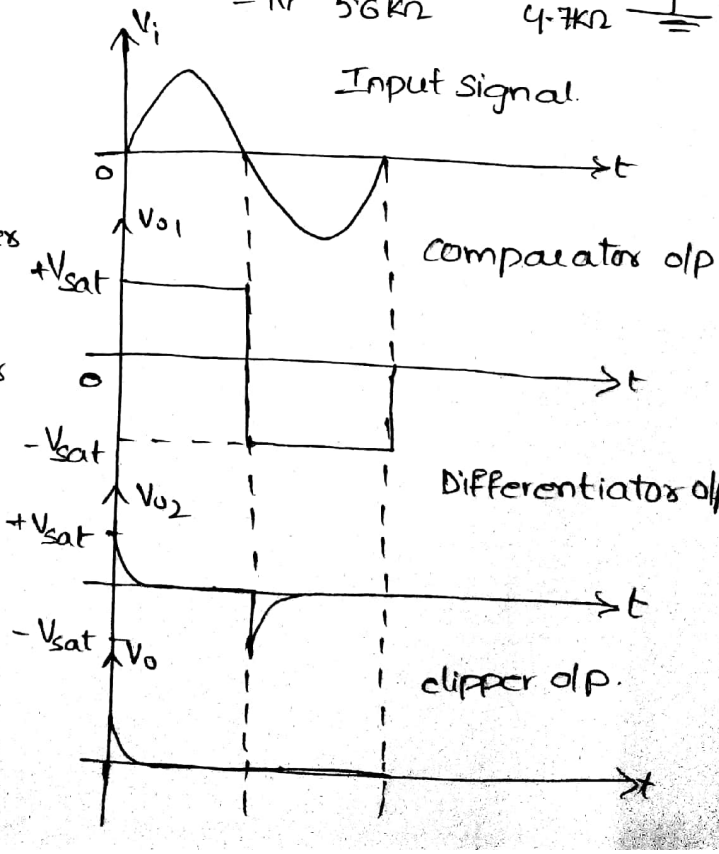
I/p voltage	Yellow	Green	Red
$V_i < 3V$	ON	OFF	OFF
$3V < V_i < 6V$	OFF	ON	OFF
$V_i > 6V$	OFF	OFF	ON



3) Time markers generators:



It is used to generate trigger signals and mainly used in one shot (or) monostable multivibrator.

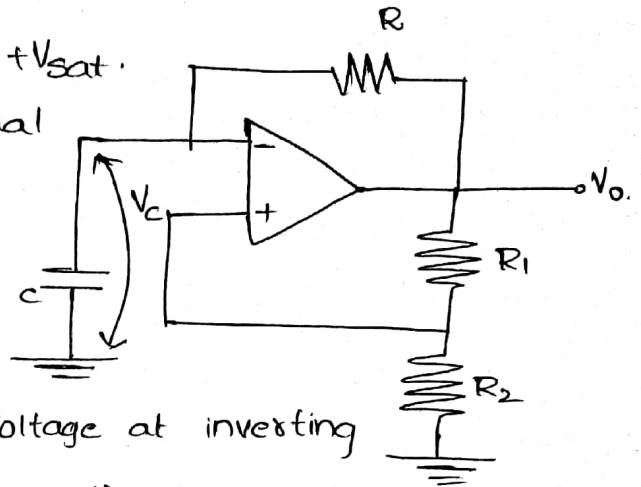


4. phase detector :- It is same as time marker generator but at the input a phase detector is used

Multivibrators :-

Astable Multivibrator :-

It is also called as square wave generator (or) free running oscillator (or) Relaxation oscillator. In this 2 quasi stable states are present and it doesn't require any triggering to change its states.

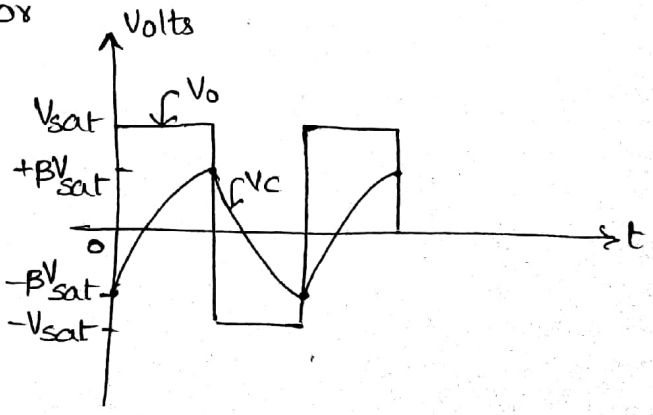


consider the output is at $+V_{sat}$. The voltage at +ve input terminal is $+\beta V_{sat}$ (β is $\frac{R_2}{R_1+R_2}$) at this instant of time, the capacitor starts charging towards to $+V_{sat}$ through the resistor R. when the voltage at inverting terminal becomes just greater than the reference voltage ($+\beta V_{sat}$) the output is suddenly drops to $-V_{sat}$. At this point, the capacitor starts discharging through resistor R of value $-\beta V_{sat}$. when the voltage at the inverting terminal becomes less than $-\beta V_{sat}$. The output is driven to +ve V_{sat} & the cycle repeats.

Frequency of Oscillations for Square wave generator :-

The voltage across the capacitor as a function of time is given as

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$



from the waveforms.,

$$V_f = +V_{sat} \qquad V_i = \beta V_{sat}$$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

$$= V_{sat}\left[\left[1 - (1+\beta)\right] e^{-t/RC}\right]$$

$$t = T_1, \quad V_c(t) = \beta V_{sat}$$

$$\beta V_{sat} = V_{sat}\left[1 - (1+\beta)\, e^{-T_1/RC}\right]$$

$$(1+\beta)e^{-T_1/RC} = 1-\beta$$

$$e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$$

$$-T_1/RC = \ln\left(\frac{1-\beta}{1+\beta}\right)$$

$$T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$T_1 = T_2$$

$$\Rightarrow T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

Assume $\beta = 0.5$, $R_1 = R_2$

$$T = 2RC \ln\left(\frac{3/2}{1/2}\right)$$

$$T = 2RC \ln(3)$$

$$T = 2.19\,RC$$

$$T \simeq 2.2\,RC$$

$$f = \frac{1}{T} = \frac{1}{2.2RC}$$

The peak to peak amplitude of square wave generator is

$$V_{o(p-p)} = 2V_{sat}$$

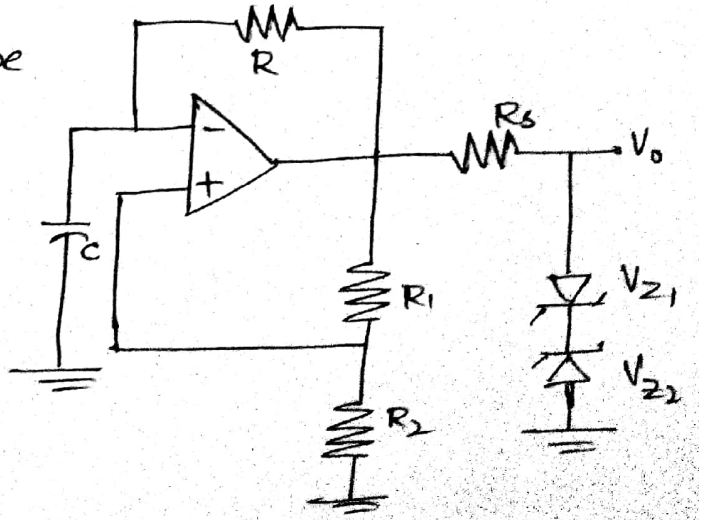
The amplitude can be varied, the power supply voltage. The peak amplitude can also be varied by making the power supply constant and the use of zener diodes connected back to back at the output. The output voltage is the summation of saturation voltage and zener break down voltage.

Symmetrical square wave can be generated if $V_{Z1} = V_{Z2}$

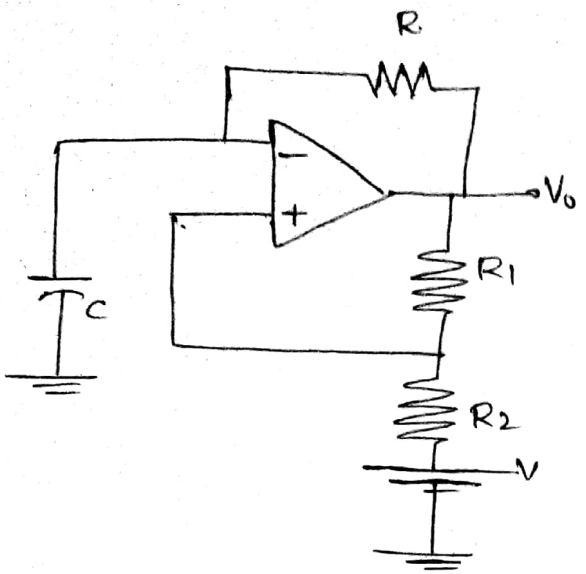
$\Rightarrow T_1 = T_2$

Asymmetrical square wave can be generated if $V_{Z1} \neq V_{Z2}$

$\Rightarrow T_1 \neq T_2$



An alternative method for generating asymmetrical square wave by using voltage to frequency converter



The capacitor charging and discharging voltages are given as:

charging voltage is $+\beta V_{sat} + V$.

discharging voltage is $-\beta V_{sat} + V$

The ON time, $T_{ON} / T_1 = RC \ln\left(\frac{1+\beta(V_{o2}/V_{o1})}{1-\beta}\right)$

The OFF time, $T_{OFF} / T_2 = RC \ln\left(\frac{1+\beta(V_{o1}/V_{o2})}{1-\beta}\right)$

Problems:-

1. Design a free running oscillator with T_{ON} of value 0.1 ms and T_{off} is 0.2 ms.

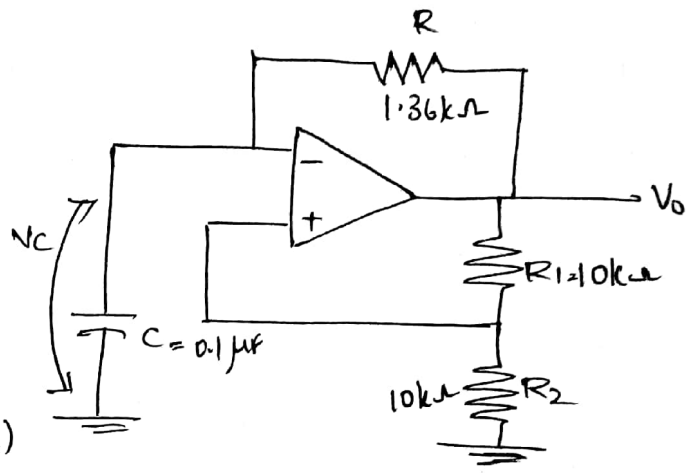
Sol:- Given $T_{ON} = 0.1 ms$

$T_{OFF} = 0.2 ms$

$T = T_{ON} + T_{off}$

$T = 0.1 + 0.2 = 0.3 ms$

Assume $\beta = 0.5$ $(R_1 = R_2)$



let $R_1 = 10K\Omega$. $\Rightarrow R_2 = 10K\Omega$

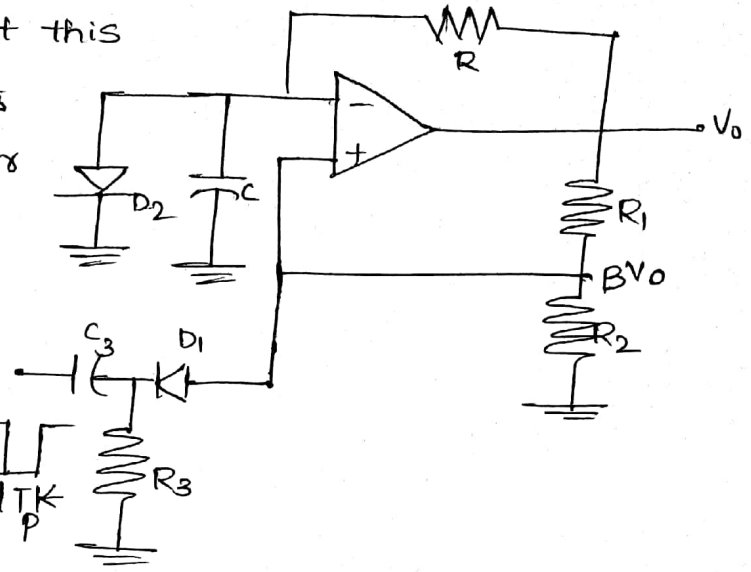
$T = 2.2RC \Rightarrow C \leq 1\mu F \Rightarrow C = 0.1\mu F$

$0.3 \times 10^{-3} = 2.2 \times R \times 0.1 \times 10^{-6}$

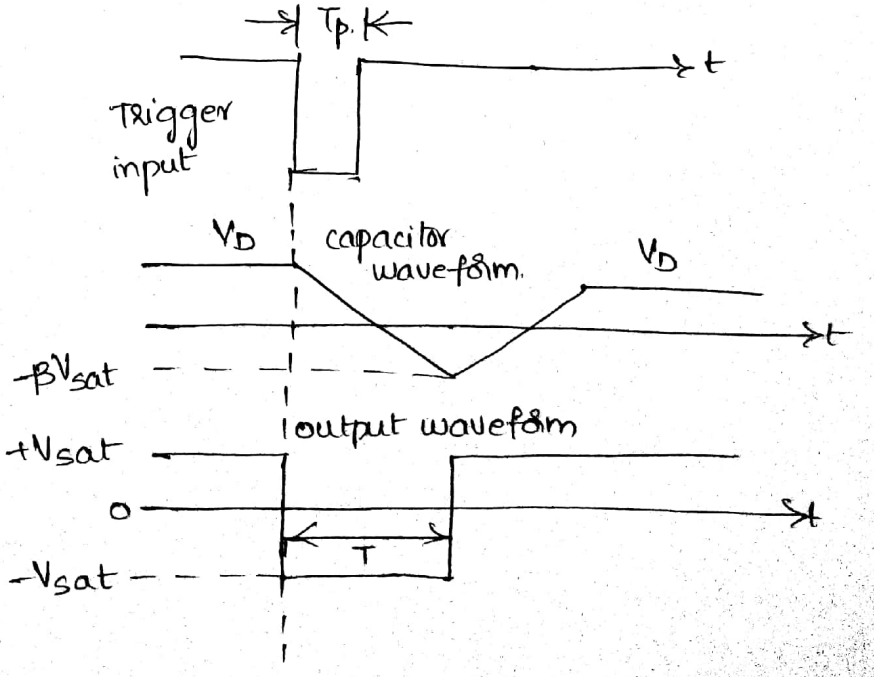
$R = 1.36\ K\Omega$

Monostable Multivibrator:-

It is also called as one shot multivibrator delay circuit (or) gating circuit It needs one trigger pulse to change its state. The monostable multivibrator is used in sampling gates.



Consider V_o is $+V_{sat}$. At this instant the capacitor starts charging when the capacitor voltage reaches to 0.7V. The diode D_2 will go ON implies V_c is clamped to 0.7V. A negative trigger pulse is applied at the non-inverting terminal of op-amp whose voltage is $\beta V_{sat} - V_1$ which is always 0.7V. Hence the output of op-amp will switch from $+V_{sat}$ to $-V_{sat}$. Due to this the diode D_2 will be in reverse bias & the capacitor starts discharging to $-V_{sat}$ through the resistor R. If the voltage at non-inverting terminal is high compared to inverting terminal. The output of op-amp again switches from $-V_{sat}$ to $+V_{sat}$ and the cycle repeats.



Expression for pulse width:-

The voltage across capacitor is $V_c(t) = V_f + (V_i - V_f)e^{-t/RC}$

from the waveform, $V_f = -V_{sat}$ $V_i = V_D$

$$V_c(t) = -V_{sat} + (V_D + V_{sat})e^{-t/RC}$$

At $t = T$, $V_c(t) = -\beta V_{sat}$

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

$$-\beta V_{sat} = V_{sat}\left[-1 + \left(\frac{V_D}{V_{sat}} + 1\right)e^{-T/RC}\right]$$

$$-\beta = -1 + \left(\frac{V_D}{V_{sat}} + 1\right)e^{-T/RC}$$

$$1 - \beta = \left(1 + \frac{V_D}{V_{sat}}\right)e^{-T/RC}$$

$$e^{T/RC} = \frac{(1 + (V_D/V_{sat}))}{1-\beta}$$

$$\frac{T}{RC} = \ln\left[\frac{1 + (V_D/V_{sat})}{1-\beta}\right]$$

$$T = RC \ln\left[\frac{1 + (V_D/V_{sat})}{1-\beta}\right]$$

$V_D = 0.7V$; $V_{sat} = 15V$

$$\frac{V_D}{V_{sat}} = \frac{0.7}{15} = 0.046 < 1.$$

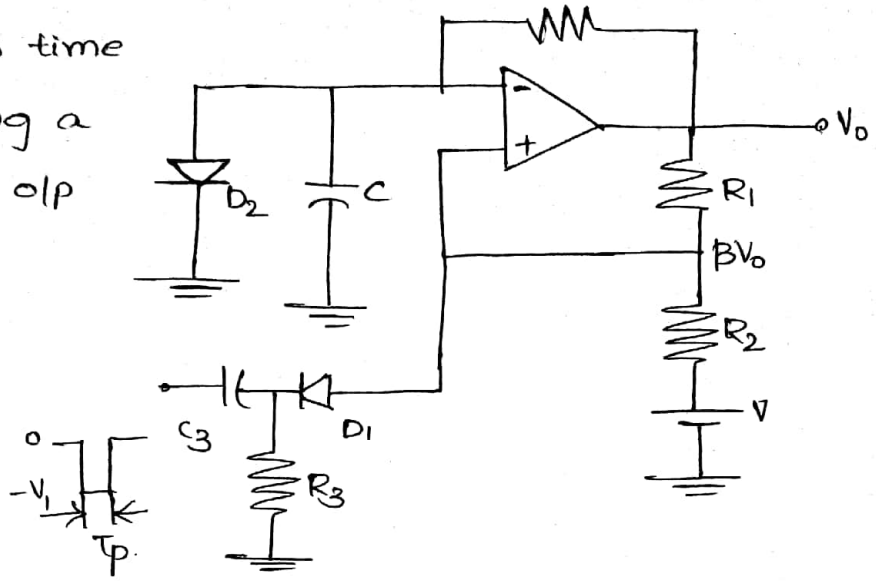
Eliminate (V_D/V_{sat}).,

$$T = RC \ln\left(\frac{1}{1-\beta}\right)$$

when $\beta = 0.5$., $T = RC \ln(2)$

$$\boxed{T = 0.693RC}$$

The monostable multivibrator can be used as voltage to time convertor by adding a dc voltage at the o/p side.



problem:-

1. Design a monostable multivibrator whose pulse width is 650 μsec, the saturation voltage is 9V, which is triggered by an input voltage & input pulse of value 3V. & the time period 50 μsec.

Sol:- Given $-V_1 = 3V \Rightarrow V_1 = -3V$

$T_p = 50\,\mu sec$

$+V_{sat} = \pm 9V$

$T = 650\,\mu sec$

$T = RC \ln\left(\frac{1}{1-\beta}\right)$

Assume $\beta = 0.5 \Rightarrow R_1 = R_2 = 10\,K\Omega$

$T = 0.693\,RC$

$650\,\mu s = T$

let $0.1\,\mu F = C$

$650\,\mu = 0.693(0.1\,\mu)R$

$$\boxed{R = 9.37\ K\Omega}$$

$R_3 C_3 < T_p$

let $\boxed{C_3 = 0.1\,\mu F}$

$R_3 < \frac{50\,\mu}{0.1\,\mu}$

$$\boxed{R_3 < 500\,\Omega}$$

Sample and Hold Analysis:- In analog to digital conversion, the analog input voltage should be held constant during the conversion cycle.

→ If the analog input voltage changes by more than $\pm\frac{1}{2}$ LSB, an error can occur in the digital output code.

→ let us consider, the analog input voltage at start of conversion process is 0V and at the end of conversion process, it is near to 1.5V. This result doesn't corresponds to the analog voltage at the start (or) at the end of conversion.

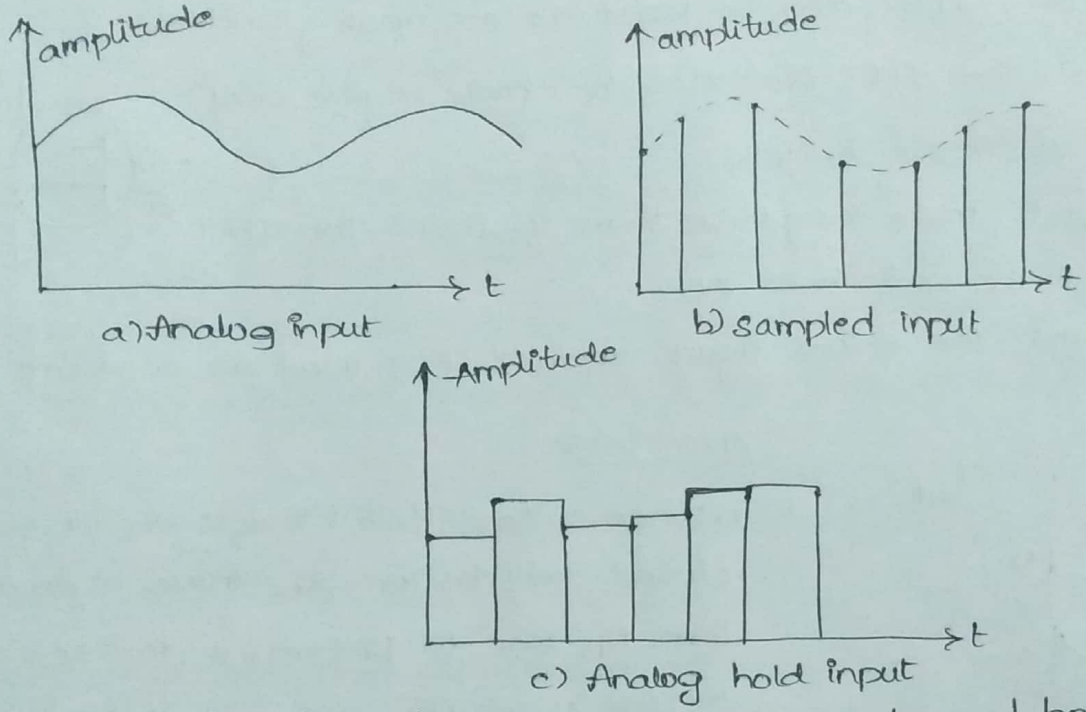
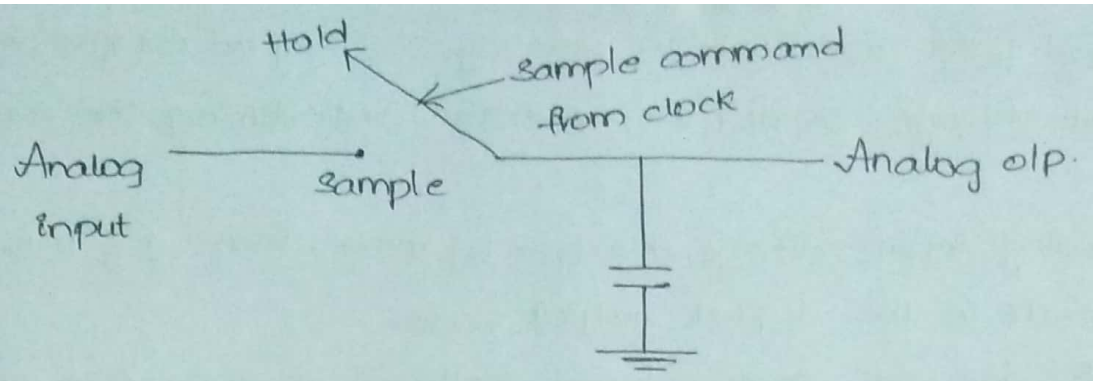


fig: I/p and o/p response of sample and hold circuit

→ To minimise the occurance of these errors, it is necessary to hold the value of analog input voltage constant during the conversion process. For this, sample and hold circuit are used.

→ The sample and hold (S/H) circuit implies, it samples the value of the input signal in response to a sampling command and hold it at the output until arrival of the next command. This is shown in fig (1).

→ The basic components used for S/H is analog switch and capacitor. The below figure shows the basic S/H circuit.

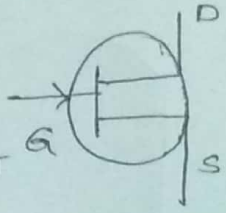


→ When the switch is closed, the capacitor charges upto the analog input voltage and when switch is open, the capacitor holds this value.

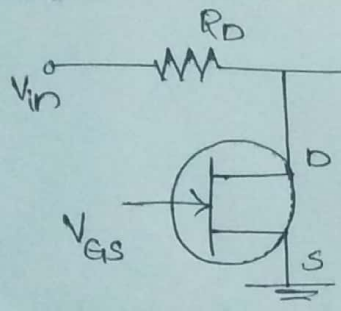
Analog switches:- JFET can be used as an analog switch.

i) when $V_{GS}=0$, the JFET operates in ohmic region and JFET act as a closed switch.

ii) when V_{GS} is more negative than $V_{GS(OFF)}$, the JFET is cut off and the switch is OFF.



a) shunt switch:- The below figure shows JFET used as a shunt switch.

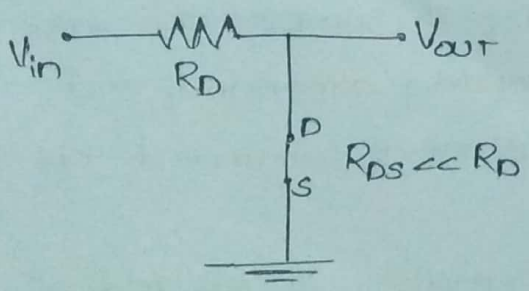


a) shunt switch

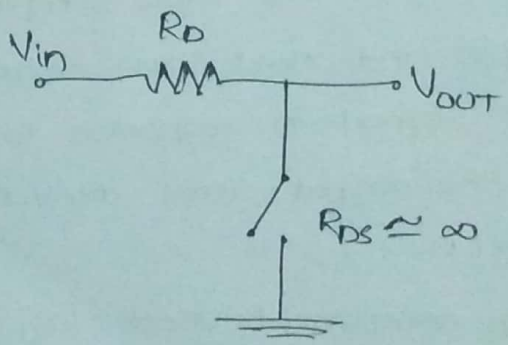
operation:-

i) when $V_{GS}=0V$, JFET acts as a closed switch. The R_{DS} value is small than R_D. Due to potential divider action, V_0 is very small and is approximately equal to 0V.

ii) when $V_{GS} \leq V_{GS(OFF)}$, JFET acts as a open switch. Due to this, $V_{OUT} = V_{in}$.

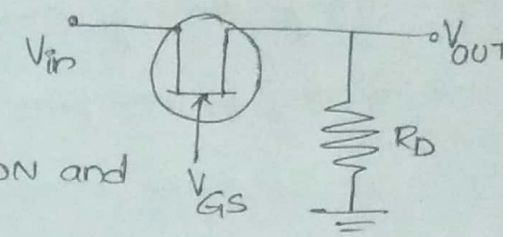


At $V_{GS}=0V$.



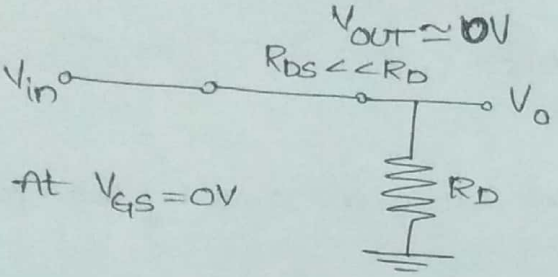
At $V_{GS} \leq V_{GS(OFF)}$.

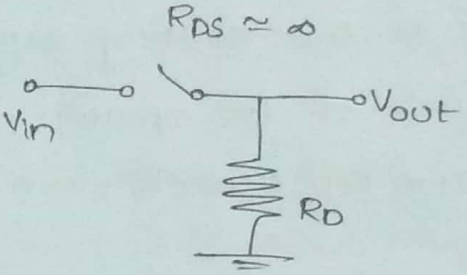
b) Series switch:- The below figure shows the JFET used as a series switch.



operation:- i) when $V_{GS} = 0V$, switch is closed and $V_{OUT} = V_{in}$

ii) when $V_{GS} \leq V_{GS(OFF)}$, switch is ON and





At $V_{GS} \leq V_{GS(OFF)}$.

Sample and Hold circuits:- Four basic sample / Hold circuits are there. In these circuits, a JFET is used as a switch.

→ During the sampling time, the JFET switch is turned on and the holding capacitor changes upto the level of the analog input voltage.

→ At the end of this sampling period, the JFET switch is turned off. As a result, the voltage across the capacitor, C_H is the output voltage and remains constant at the end of sampling time.

→ During the hold period, there (until be) will be a small drop-off in the capacitor voltage due to the various leakage currents

→ To avoid this, input and output buffer circuits are used.

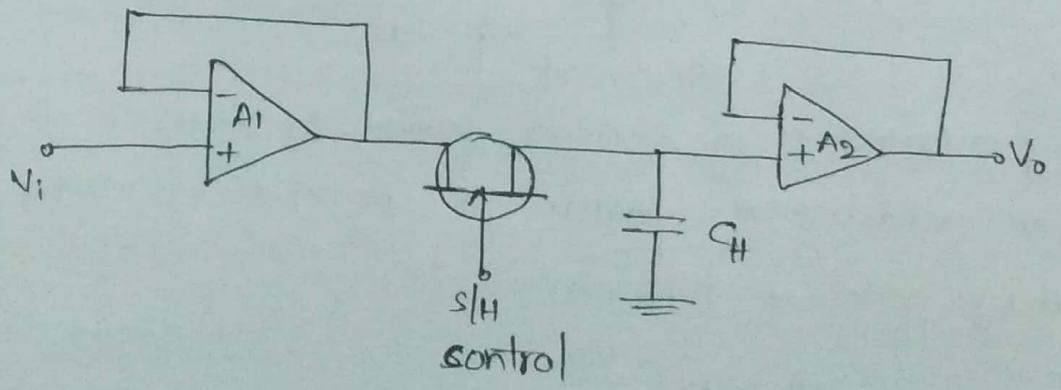


Fig. 1: Open loop S/H circuit

→ The acquisition time of a S/H circuit is the time required for the holding capacitor, C_H to charge upto a level close to the i/p voltage during sampling.

→ In fig: 1, three principle factors are,

i) RC time constant where R is r_{ds} (ON) i.e., on resistance of JFET and C is the holding capacitance, C_H.

ii) Slew rate of the op-amp.

iii) Maximum o/p current, which can be source(or) sunk by the operational amplifier.

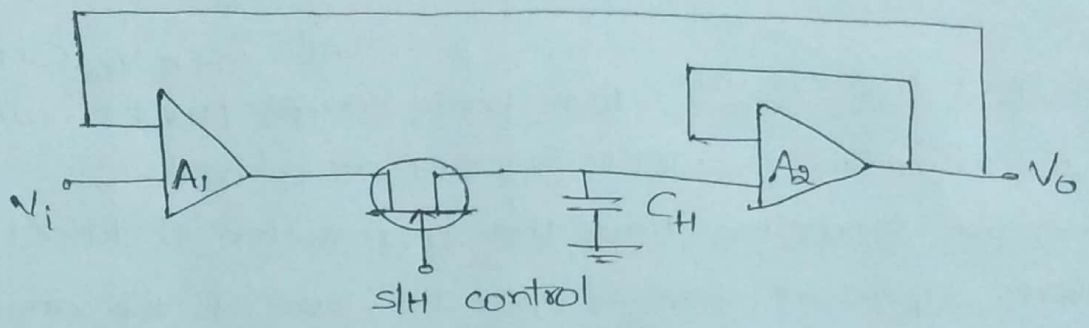
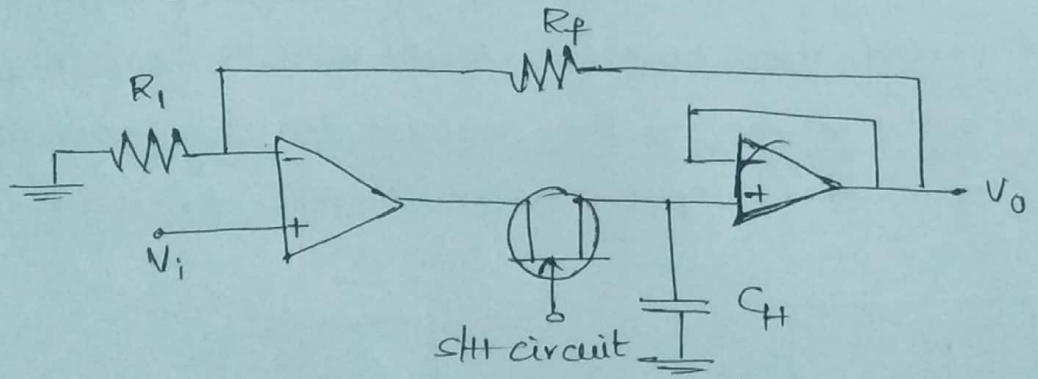


fig.2: closed loop S/H circuit.

→ In fig. 2, the acquisition time for this circuit is limited by maximum output current and slew rate of the op-amp, rather than the RC time constant.



→ Fig.3 performs in a similar fashion to that of fig. 2. Fig.3 provides an additional feature of providing voltage gain.

The voltage gain of this circuit is

$$A = 1 + \frac{R_f}{R_1}$$

→ Therefore, the sampled o/p voltage is equal to the sampled i/p voltage multiplied by the voltage gain factor of $1+(R_f/R_1)$.

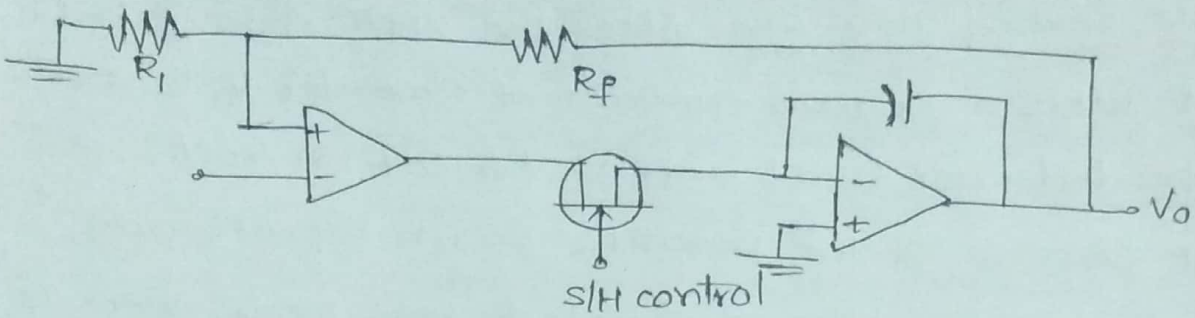


Fig.4

→ Fig.4 provides two disadvantages. The faster capacitor charging rate provides shorter acquisition time. This is because, the voltage at the inverting i/p terminal of A_2 is equal to the capacitor voltage divided by open loop gain of A_2. In this circuit, the summing i/p of A_2 remains at virtual ground.

→ Due to this, the charge removed from the summing junction via C_{gd} in constant.

→ The removed charge appears as a constant offset at the o/p However, it is constant, it can be nulled by any standard offset trimming technique.

performance parameters of S/H circuits:- The parameters are,

i) Acquisition time (t_{ac}):- It is the time required for the holding capacitor, C_H to charge upto a level close to the i/p voltage during sampling. It depends on three factors.

1) RC time constant
2) Maximum o/p current of op-amp
3) Slew rate of op-amp.

ii) Aperture time (t_{ap}):- Because of propagation delays through the driver and switch, V_o will keep tracking V_i some time after the inception of the hold command.

iii) Aperture Uncertainity (Δt_{ap}):- It is the variation in aperture time from sample to sample.

iv) Hold mode setting time (t_s):- After the application of hold command, it takes a certain amount of time for V_o to settle within a specified error band such as 1%, 0.1% (or) 0.01%.

v) Hold step:- Because of the parasitic switch capacitances, at the time of switching between sample to hold mode, there is an unwanted transfer of charge between the switch driver and C_H. This changes in o/p voltage and is referred as pedestral error. The change in output voltage is given below,

$$\Delta V_o = \frac{\Delta Q}{C_H}.$$

vi) Feed through:- In hold mode, because of stray capacitance across the switch, there is a small amount of a.c coupling between V_o and V_i. This ac coupling causes output voltage to vary with variation in input voltage. This is referred as feed through and is given as,

$$\Delta V_o \cong \frac{C_{ds}}{C_H} \Delta V_i$$

→ Feed through is usually expressed in terms of feedthrough rejection ratio, FRR and is given as,

$$\boxed{FRR = 20 \log \frac{\Delta V_i}{\Delta V_o}}$$

Problem:- Calculate the change in o/p voltage if i/p changes by 5V with FRR for S/H circuit is 80dB.

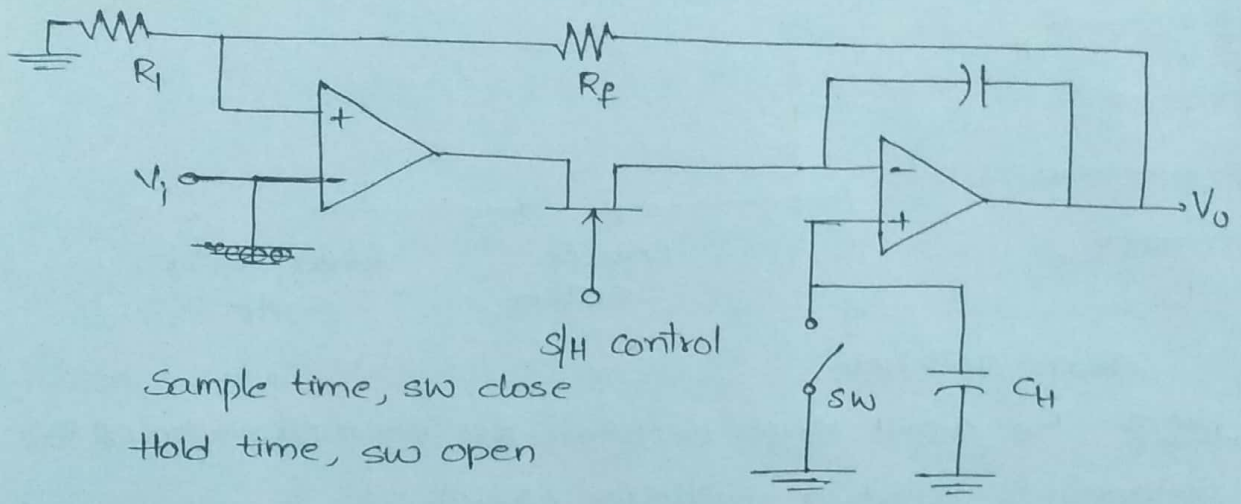
Sol:- W.K.T., $FRR = 20 \log_{10} \frac{\Delta V_i}{\Delta V_o}$.

Given $\Delta V_i = 5V$

$$80 = 20 \log_{10} \frac{5}{\Delta V_o}$$

$$\Delta V_o = 0.5 \text{ mV}$$

Voltage drop:- The leakage current causes voltage of the capacitor to drop down. This is referred to as voltage drop. The rate of (22) which the capacitor voltage drops is known as voltage drop rate (or) drop rate. The main source of leakage current is the integrator's i/p bias current. This leakage current (voltage drop) can be reduced by connecting the non-inverting input of the integrator to a dummy capacitor, C of size equal to C_H during the hold period. The circuit diagram is shown below.



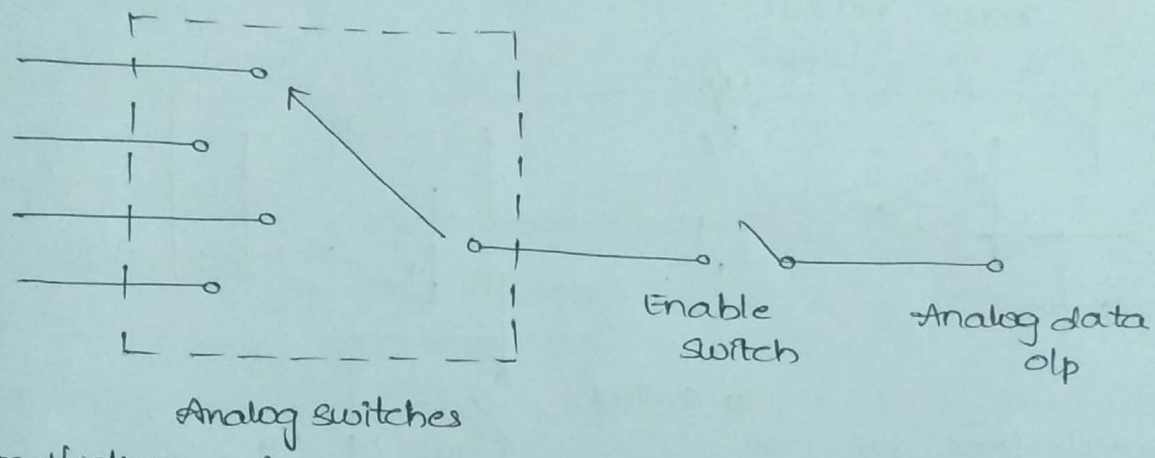
Advantages of S/H circuits:-

1. It is used to reduce the cross talk in the multiplexer.
2. In case of multichannel ACD's, synchronizer can be achieved by sampling signals from all channels at the same time.
3. Its primary use is, to hold the sampled analog i/p voltage constant during conversion time of A/D converter.

Applications of S/H circuits:-

1. Digital interfacing
2. ACD's
3. pulse modulation systems
4. Analog Demultiplexers.

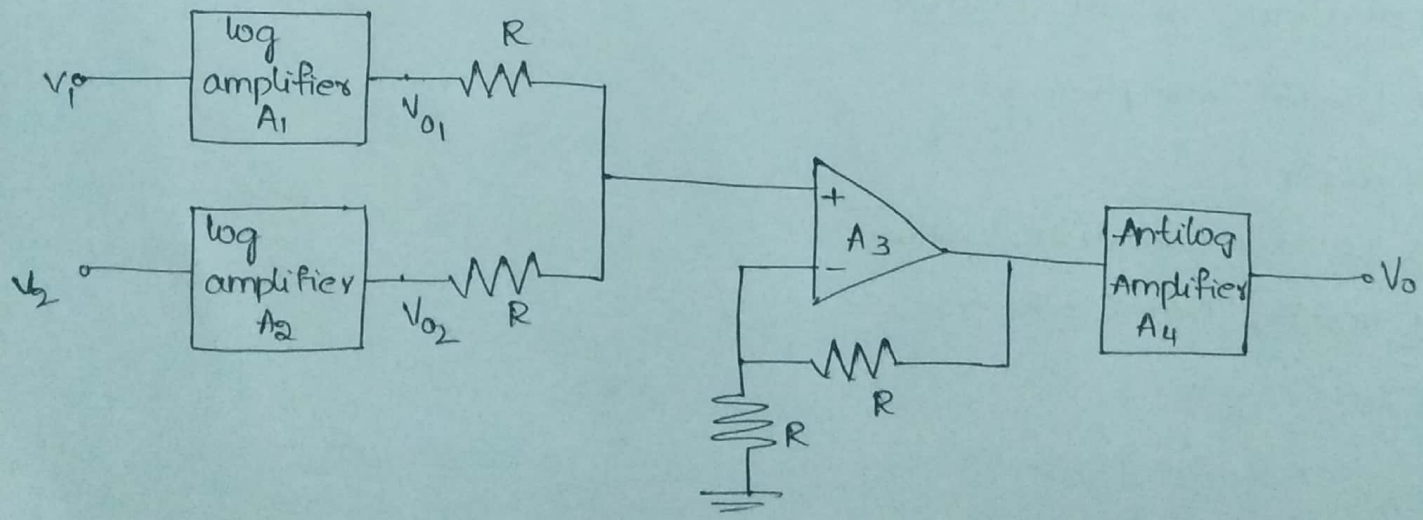
Analog multiplexer:- It is similar to digital multiplexer except analog i/p's are multiplexed instead of digital i/ps. It allows analog ~~i/f~~ information from several sources to be routed onto a single output line. This is shown in below figure. The selection of a particular i/p line is controlled by a set of selection lines. There are 2^n input lines and n selection lines whose bit combinations determines which i/p is selected.



Analog multipliers:- The circuit which performs the multiplication of the two input voltages is called a multiplier circuit.

→ Such multiplier circuits are used in the various variety of applications such as squarer, square root extracter, frequency doubler, etc.

Analog Voltage Multiplier circuit:- Using log, adder and anti-log amplifiers, the circuit can be built to obtain the output proportional to the product of two input voltages. The circuit is called analog voltage multiplier and is shown below.



Analog voltage divider circuit :- Analog voltage divider can be

Circuit Analysis :-

The log amplifier circuits with A_1, A_2 give the outputs as V_{o1} and V_{o2} and is given as,

$$V_{o1} = K_1 \ln (K_2 V_1) \longrightarrow (1)$$

$$V_{o2} = K_2 \ln (K_2 V_2) \longrightarrow (2)$$

where $K_1 = \dfrac{-V_T (R_2 + R_{TC})}{R_{TC}}$ and $K_2 = \dfrac{1}{V_{ref}}$

Now, op-amp A_3 is non-inverting summer (with equal R), the o/p voltage, V_{o3} is given as,

$$V_{o3} = V_{o1} + V_{o2} = K_1 \ln(K_2 V_1) + K_2 \ln (K_2 V_2)$$

$$V_{o3} = K_1 \ln (K^2 V_1 V_2) \quad (\because \log ab = \log a + \log b)$$

→ Now V_{o3} is applied as i/p to antilog amplifier, A_4. The o/p voltage V_o is given as,

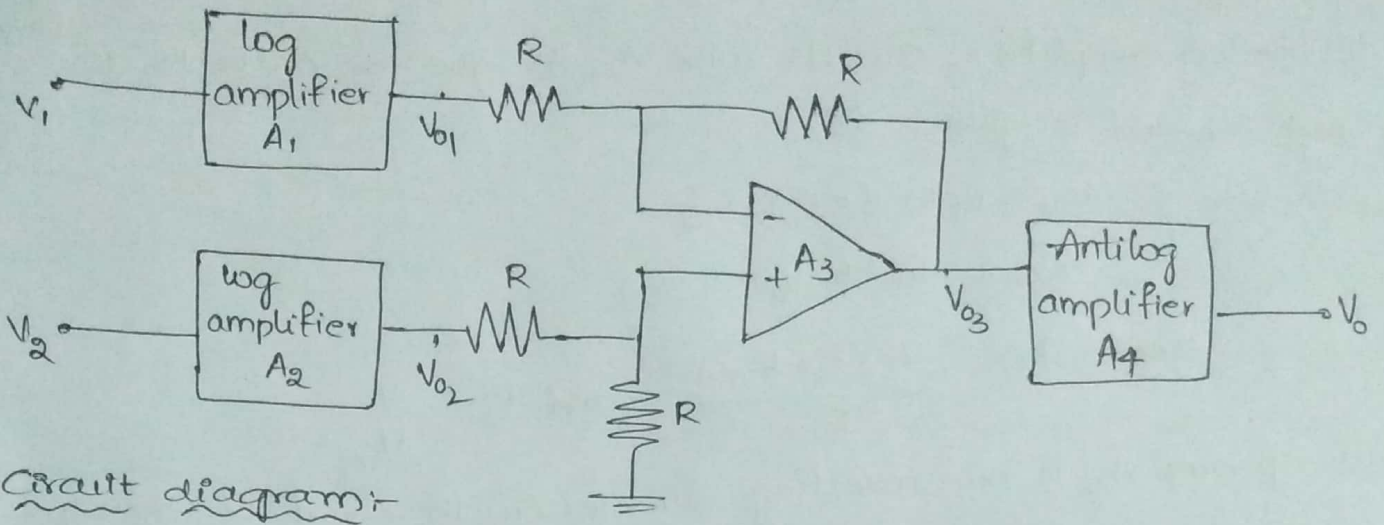
$$V_o = \frac{1}{K_2} \ln^{-1} \left[\frac{K_1 \ln (K_2^2 V_1 V_2)}{K_1} \right]$$

$$V_o = \frac{1}{K_2} K_2^2 V_1 \cdot V_2$$

$$\boxed{V_o = K_2 V_1 V_2}$$

Thus, the o/p is proportional to the product of two analog inputs V_1 and V_2.

Analog Voltage divider circuit :- Analog voltage divider can be obtained using log and antilog amplifiers. This circuit gives o/p which is proportional to the division of the two i/p signals. The circuit diagram is shown below:



Circuit diagram:-

V_{o1} and V_{o2} are the o/p voltage of the log amplifiers circuits for the i/p signals V_1 and V_2,

$$\therefore V_{o1} = K_1 \ln(K_2 V_1)$$

$$V_{o2} = K_2 \ln(K_2 V_2)$$

where $K_1 = \dfrac{-V_T(R_2+R_{TC})}{R_{TC}}$; $K_2 = \dfrac{1}{V_{ref}}$

Now, op-amp A_3 is subtractor and is given as,

$$V_{o3} = V_{o2} - V_{o1} = K_1 \ln(K_2 V_2) - K_1 \ln(K_2 V_1)$$

$$V_{o3} = K_1 \ln(V_2/V_1)$$

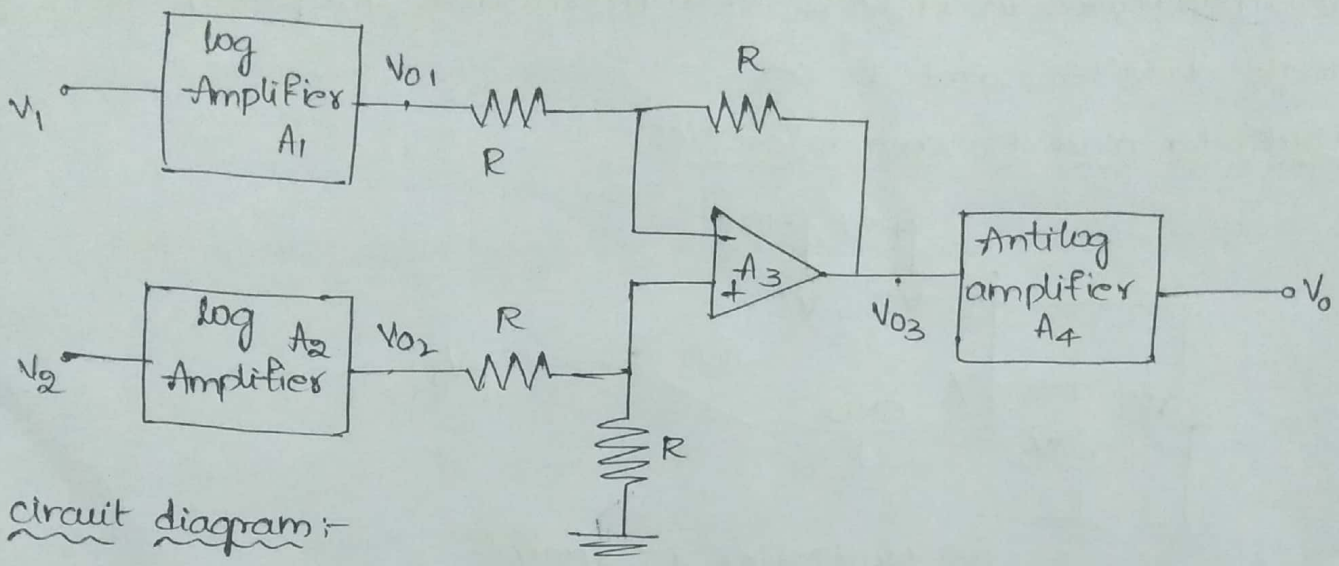
→ Now, V_{o3} is applied as i/p to the antilog amplifier and is given as

$$V_o = \frac{1}{K_2} \ln^{-1}\left[K_1 \cdot \frac{\ln(V_2/V_1)}{K_1}\right]$$

$$= \frac{1}{K_2} \cdot \frac{V_2}{V_1}$$

∴ The o/p is proportional to the division of two analog inputs V_1 and V_2.

Analog voltage divider circuit :- Analog voltage divider can be obtained using log and antilog amplifiers. This circuit gives o/p which is proportional to the divider to the two input signals. The circuit diagram is shown below:



circuit diagram :-

V_{o_1} and V_{o_2} are the o/p voltages of the log amplifier circuits for the i/p signals V_1 and V_2.

$$V_{o_1} = K_1 \ln(K_2 V_1) \qquad V_{o_2} = K_1 \ln(K_2 V_2)$$

where $K = \dfrac{-V_T (R_2 + R_{TC})}{R_{TC}}$; $K_2 = \dfrac{1}{V_{ref}}$

Now, op-amp, A_3 is subtractor and is given as

$$V_{o_3} = V_{o_2} - V_{o_1} = K_1 \ln(K_2 V_2) - K_1 \ln(K_2 V_1)$$

$$V_{o_3} = K_1 \ln(V_2/V_1)$$

Now, V_{o_3} is applied as o/p to the antilog amplifier and is given as,

$$V_o = \frac{1}{K_2}\left[\ln^{-1}\left(K_1 \frac{\ln(V_2/V_1)}{K_1}\right)\right] = \frac{1}{K_2} \cdot \frac{V_2}{V_1}$$

∴ The o/p is proportional to the division of two analog i/p's V_1 & V_2.

Multiplier Integrated Circuit:- Instead of using voltage multiplier circuit, the multiplier IC is commonly used.

→ Monolithic integration has lowered the cost of multiplier IC's.

→ These ICs can be configured to use in many applications as signal multiplications in process instrumentation, frequency doublers, phase angle detectors and so on.

Basic Multiplier and its characteristics:-

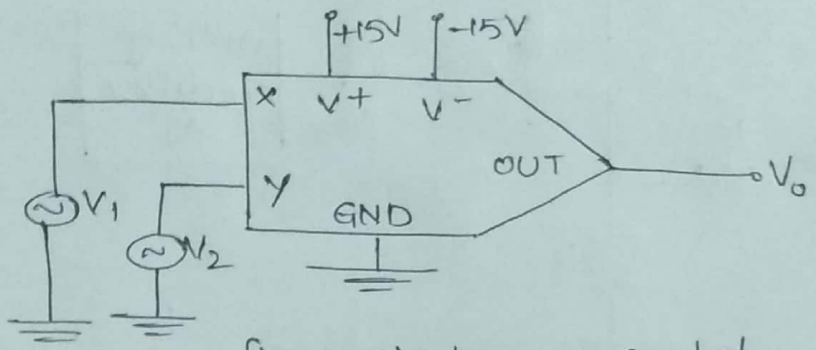


fig: Multiplier IC symbol.

→ A basic multiplier is an active circuit in which the output voltage is proportional to the product of the two input signals. The symbol is shown in above figure.

→ The terminals V+, V- are supply terminals of IC. X and Y are the two input terminals in which 2 i/p's V_1 and V_2 are connected.

→ The o/p of such basic multiplier is,

$$V_o = K V_1 V_2$$

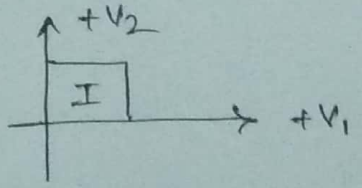
where K is constant, $K = \frac{1}{V_{ref}}$.

$$V_o = \frac{V_1 V_2}{V_{ref}}$$

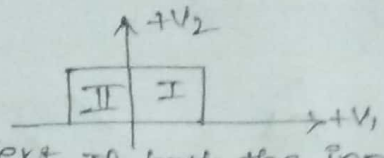
Internally, $V_{ref} = 10$, $V_o = \frac{V_1 V_2}{10}$

→ Depending on the polarity restriction, the IC operation is called as

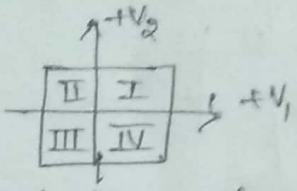
i) one quadrant multiplier:- In such operations, the polarities of both i/ps must always be positive.



(ii) Two quadrant multiplier:- In this, one i/p is held positive and the other is allowed to swing in both positive and negative.



(iii) Four quadrant multiplier:- If both the inputs are allowed to swing in both positive and negative directions, the operation is said to be four quadrant multiplier.



Performance parameters of multipliers:- The performance parameters of a multiplier are:

1. Accuracy:- It is the maximum deviation of the actual o/p level from the ideal one. This deviation is also called as total error. It is generally specified interms of percentage of full scale output.

2. Linearity:- It is the maximum o/p deviation from the best fit straight line at the o/p, where one i/p is varied and the other is kept fixed.

3. Bandwidth:- It is the range upto the frequency where the o/p is 3dB below its low frequency value.

4) 1% absolute error bandwidth:- It represents the frequency where the o/p magnitude starts to deviate from its low frequency by 1%.

5) Feed through voltage:- It is the peak to peak voltage at the o/p when the one of the two inputs is grounded.

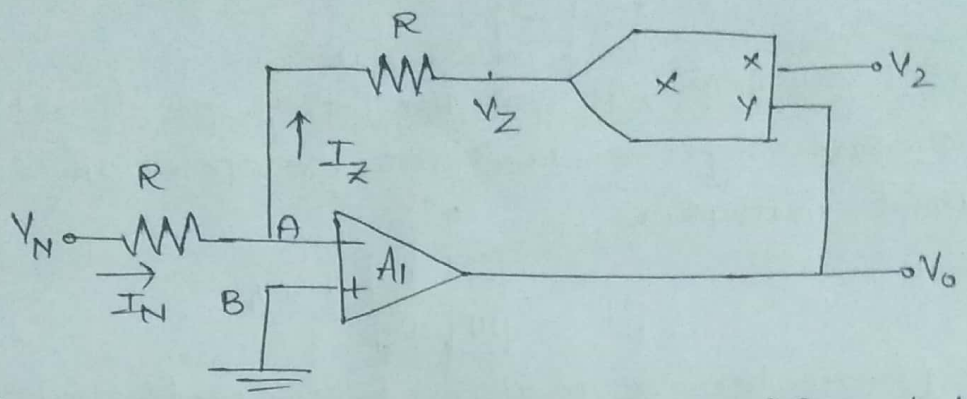
6) Zero trim:- It is the ability of the multiplier to set the feed through voltage at the o/p to zero.

7) Scale factor:- It is the proportionality constant (K) relating the o/p voltage and the product of two i/p voltages.

$$K = \frac{V_o}{V_1 \cdot V_2}$$

Applications of Multiplier: Some of the applications are:

a) Voltage divider using Multiplier:



→ The circuit in which the output is the division of two i/p signals is called as a voltage divider. The circuit is shown above.

→ The multiplier is used in feedback loop. The denominator is applied at the x i/p of the multiplier which is V_2. The numerator is applied at the input terminal of op-amp A_1.

→ As node B is grounded, node A is also grounded according to virtual ground i.e., $V_A = 0$

$$\text{Now., } I_N = \frac{V_N}{R} = \frac{-V_Z}{R}$$

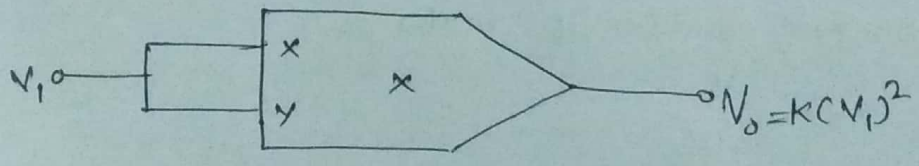
$$\text{W.K.T., } V_Z = K V_1 V_2 = K V_o V_2.$$

$$\Rightarrow \frac{V_N}{R} = \frac{-K V_o \cdot V_2}{R}$$

$$V_o = \frac{-V_N}{K V_2}$$

∴ The o/p is proportional to the division of 2 i/p voltages V_N and V_2.

b) Squaring circuit using Multiplier:



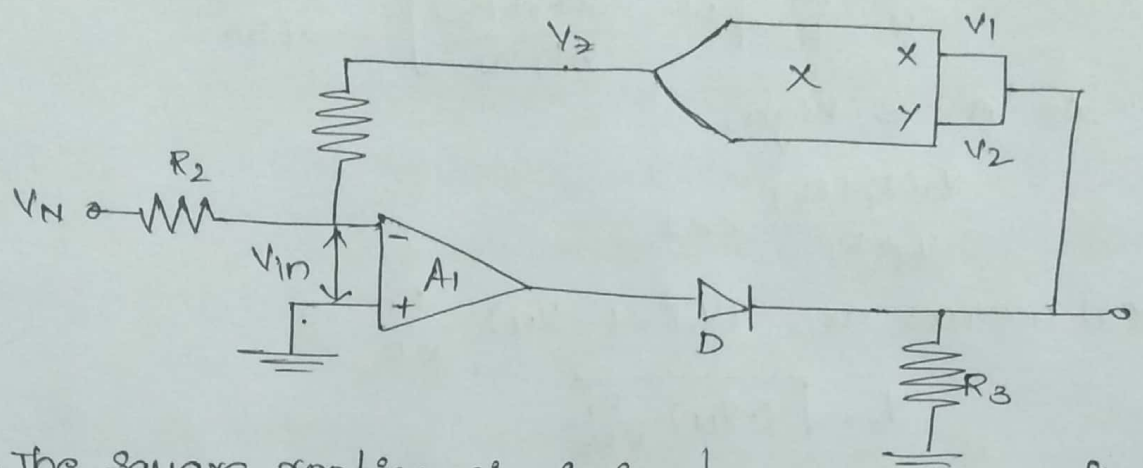
→ The Squaring circuit gives square of the i/p voltage divider applied, the circuit is shown in above figure. In this, the i/p signal V_1 is applied to both the i/p terminals of the multiplier.

As $V_1 = V_2$

$$V_o = K V_1 V_2 = K(V_1)^2$$

∴ o/p is proportional to the square of the i/p.

c) Square rooting circuit using multiplier:



→ The square rooting circuit is shown in above figure. A multiplier configured as squaring circuit is used in the feedback loop. The gain of the op-amp A_1 is say A and voltage between inverting and non-inverting terminal is V_{in}.

We can write, $V_o = -V_{in} A$

$$V_{in} = -\frac{V_o}{A} \rightarrow (1)$$

Take nodal equation at -ve terminal of A_1 is

$$\frac{V_{in} - V_N}{R_2} + \frac{V_{in} - V_2}{R_1} = 0$$

$$\frac{V_{in}}{R_2} + \frac{V_{in}}{R_1} = \frac{V_N}{R_2} + \frac{V_2}{R_1}$$

$$V_{in} = V_N \frac{R_1}{R_1 + R_2} + V_2 \cdot \frac{R_2}{R_1 + R_2} \rightarrow (2)$$

W.K.T., $V_2 = K V_1 V_2 = K(V_o)^2$

Substitute V_2 in eq.(2).,

$$V_{in} = V_N \cdot \frac{R_1}{R_1+R_2} + K(V_0)^2 \cdot \frac{R_2}{R_1+R_2}$$

$$\frac{-V_0}{A} = V_N \cdot \frac{R_1}{R_1+R_2} + K(V_0)^2 \cdot \frac{R_2}{R_1+R_2}$$

$$(V_0)^2 = \frac{\left(\frac{-V_0}{A} - V_N \cdot \frac{R_1}{R_1+R_2}\right)}{K} \cdot \frac{(R_1+R_2)}{R_2}$$

$$(V_0)^2 = -\frac{V_N}{K} \cdot \frac{R_1}{R_2}\left[1 + \frac{V_0(R_1+R_2)}{AR_1V_N}\right] \longrightarrow (3).$$

As 'A' is high,

$$\frac{V_0(R_1+R_2)}{V_N A R_1} << 1$$

Eq.(3) becomes as., $(V_0)^2 = (-V_N) \cdot \frac{R_1}{KR_2}$

$$V_0 = \sqrt{(-V_N) \cdot \frac{R_1}{KR_2}}$$

V_N must always be negative.

d) frequency doubler using multiplier :- The multiplication of two sine waves of same frequency but with different amplitude and phases.

consider the two input signals as,

$$V_1 = V_m \sin \omega t ; \quad V_2 = V_{2m} \sin(\omega t + \theta)$$

when two inputs are given to the multiplexer, we get

$$V_0 = K V_1 V_2$$

$$= K V_{1m} \sin \omega t \sin(\omega t + \theta) \quad V_{2m} = V_{1m} V_{2m} K \sin \omega t (\sin \omega t \cos\theta + \sin\theta \cos \omega t)$$

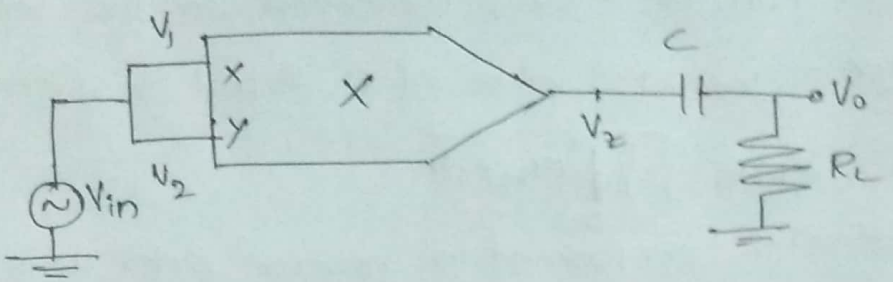
$$= K V_{1m} V_{2m} [\sin^2 \omega t \cos\theta + \sin \omega t \cos \omega t \sin\theta]$$

$\sin 2\theta = 2 \sin\theta \cos\theta$; $\sin^2 \omega t = \frac{1-\cos 2\omega t}{2}$

$$= K V_{1m} V_{2m} \left[\left(\frac{1-\cos 2\omega t}{2}\right)\cos\theta + \frac{\sin 2\omega t}{2} \cdot \sin\theta\right]$$

$$V_0 = \underbrace{\frac{K V_{1m} V_{2m} \cos\theta}{2}}_{\text{DC term}} - \underbrace{\frac{K V_{1m} V_{2m}}{2} \cos(2\omega t - \theta)}_{\text{frequency term}}$$

The frequency doubler circuit can be obtained by using a squaring circuit which is shown below



The two inputs are connected together, $V_1 = V_2 = V_{in} = V_m \sin \omega t$

$\therefore V_2$ is o/p of the multiplier,

i.e, $V_2 = KV_1V_2 = K(V_{in})^2$

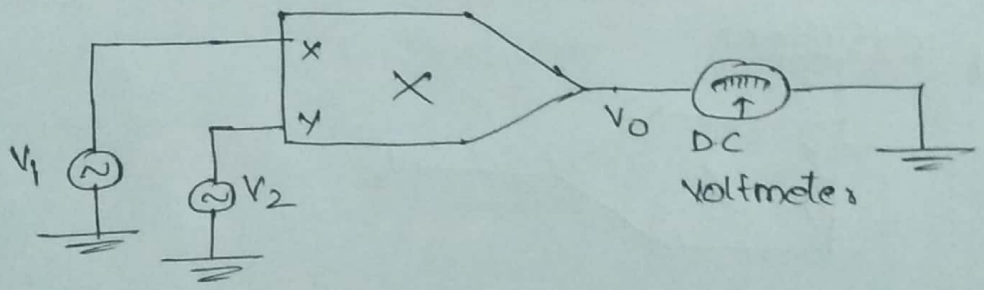
$$V_2 = KV_m^2 \sin^2 \omega t = KV_m^2 \left(\frac{1-\cos 2\omega t}{2}\right)$$

$$V_2 = \frac{KV_m^2}{2} - \frac{KV_m^2}{2} \cos 2\omega t$$

The capacitor C connected in series with the o/p blocks the DC and removes it. Thus, we get

$$\boxed{V_o = -\frac{KV_m^2}{2} \cos 2\omega t}$$

e) Phase angle detection using multiplier:- In this the two input signals have same frequency but with different amplitudes and phases. The circuit is shown below.



W.K.T, from frequency doubler, the o/p of multiplier is

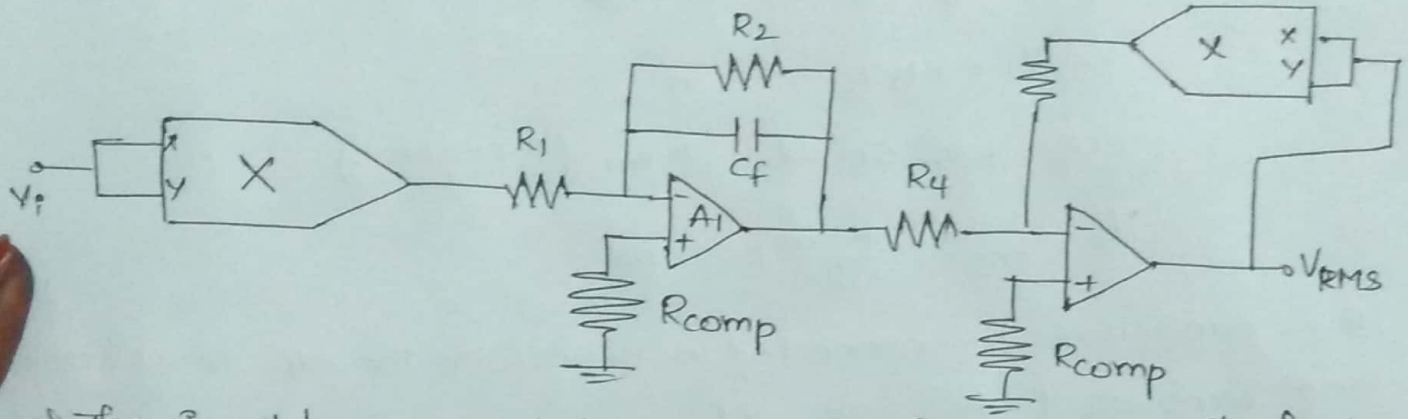
$$V_o = \frac{KV_{1m}V_{2m}\cos\theta}{2} - \frac{KV_{1m}V_{2m}}{2} \cos(2\omega t - \theta)$$

Now, the DC voltmeter is connected at the o/p. The voltmeter will not respond to ac component present in the o/p, while the dc component can be easily measured on the voltmeter.

f) RMS Detector:- The RMS value of a signal is given by

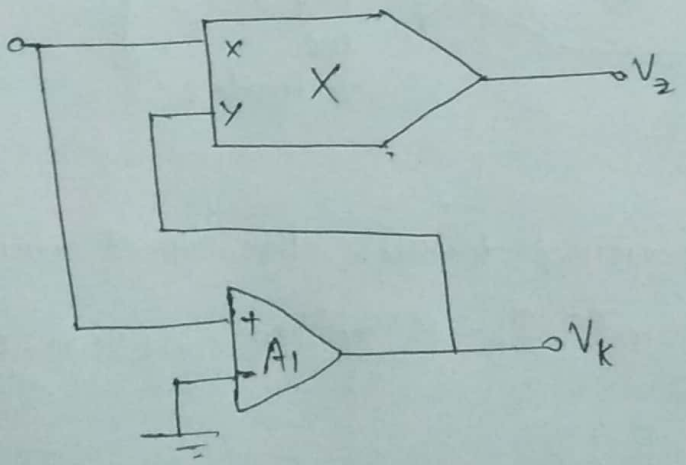
$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T (V_{in})^2 dt}$$

The operation is performed in reverse order as squaring, integrating and finally finding the square root. The below shows the basic circuit of the RMS detector.

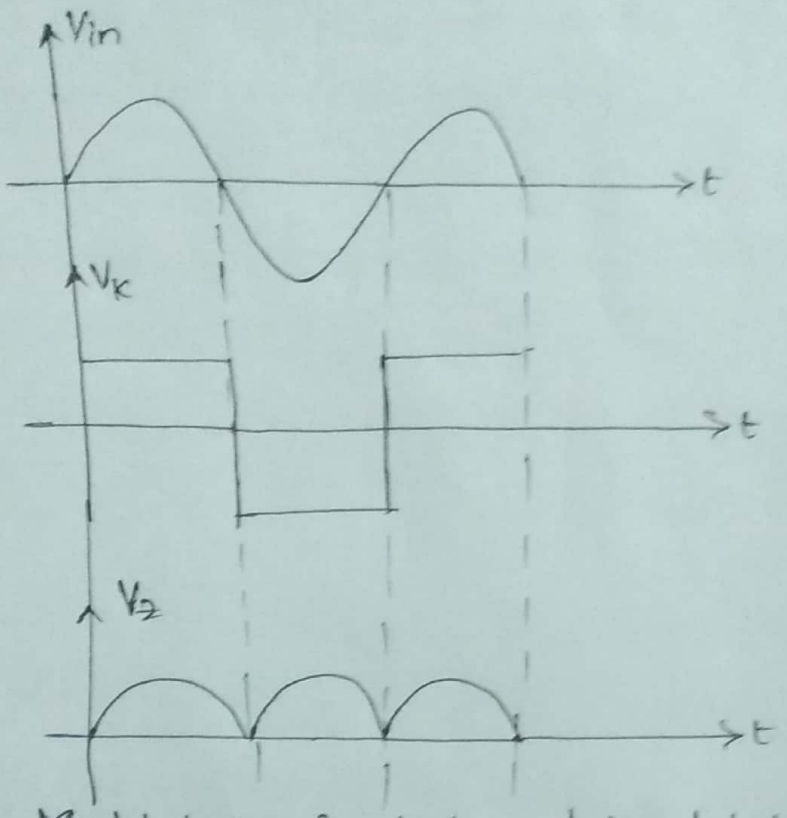


→ The circuit has a multiplier as a squaring device as its first element. This gives square of the i/p. The op-amp, A_1 is an integrator which gives the integration of squared input. finally, op-amp A_2 along with the multiplier in its feedback loop performs square rooting operation, on the o/p of op-amp. Thus, the final o/p is the RMS value of the i/p applied.

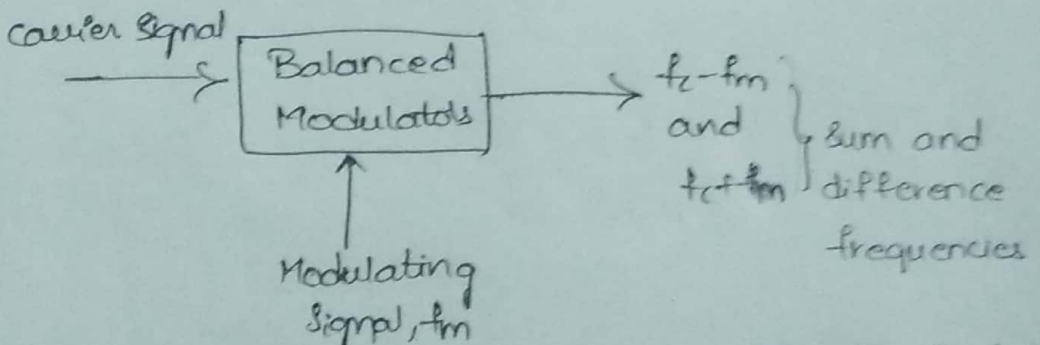
g) Rectifier using multiplier:-



full wave rectifier using multiplier is shown in above figure. the op-Amp A_1 is used as a non-inverting comparator. the o/p of op-amp A_1 is V_k and which is at $\pm V_{sat}$ depending upon whether the i/p V_{in} is +Ve/-Ve.



Balanced Modulators:- The balanced modulator accepts two signals with different frequencies. One of them is a carrier signal and other is a modulating signal. The balanced modulator produces sum and difference of these input frequencies



principle used in Balanced Modulator:- when two signals at different frequencies are passed through a non-linear resistance, the AM signal is generated with suppressed carrier. A device having

UNIT-4

ACTIVE FILTERS

Filters:- An electronic filter is often a frequency selective circuit that passes a specified band of frequencies and blocks (or) attenuates a signals of frequencies outside this band.

Classification of filters:-

1) By depending upon the type of signal, filters can be classified as,

a) Analog filters b) Digital filters.

Analog filters are designed to process analog signals. Digital filters are designed to process analog signals using digital techniques.

2) By depending upon the type of elements used, again filters are classified as,

a) passive filters b) Active filters

Elements used in passive filters are resistors, capacitors, inductors. Active filters uses transistors, op-amp in addition to resistors and capacitors.

3) By depending upon the operating frequency, this filters are again divided into two types.

a) Audio frequency (AF) b) Radio frequency (RF)

RC filters are commonly used for audio (or) low frequency operations where as LC (&) crystal filters are commonly used RF (or) high frequencies

Advantages of Active filters over passive filters:-

a) **Gain and frequency adjustment flexibility:-** Since op-amp is capable of providing a very high gain and also the input signal is not attenuated as it is in a passive filters.

b) **No Loading problem:-** Because of high i/p impedance and low output impedance of the op-amp, the active filter doesn't cause loading of the source (&) load.

→ The inductors are absent in the active filters, hence the modern active filters are more economical.

→ Active filters can be realized under number of class of functions such as Butterworth, Thomson, chebyshev, cauer, etc.

Disadvantages of active filters over passive filters:-

1) The frequency response is limited by gain bandwidth (GBW) product and slew rate of the op-amp.

2) The high frequency active filters are more expensive than passive filters.

Applications of active filters:-

Active filters are used in the following

a) Radio b) Television c) Telephone

d) Space satellite e) Bio-medical equipments

Most commonly used filters are -

1) Low pass filter (LPF)

2) High pass filter (HPF)

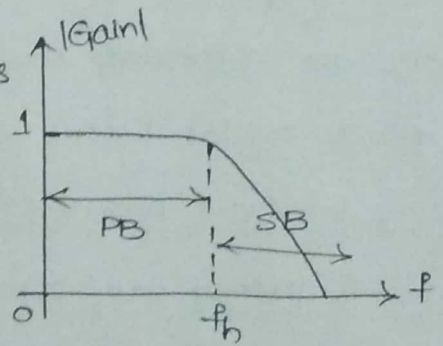
3) Band pass filter (BPF)

4) Band Reject (Band stop / Band Elimination / Notch filter)

5) All pass filter

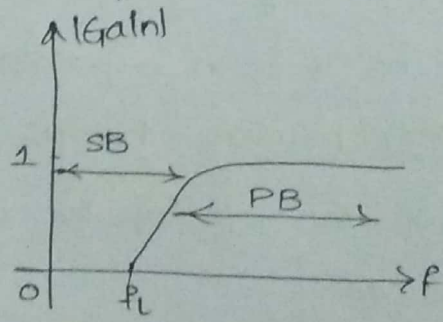
1) Low pass filter:- The frequency response of ideal LPF is

The pass band allows the frequencies which are in the range of 0 to f_h and the stop band rejects the frequencies that are greater than f_h.



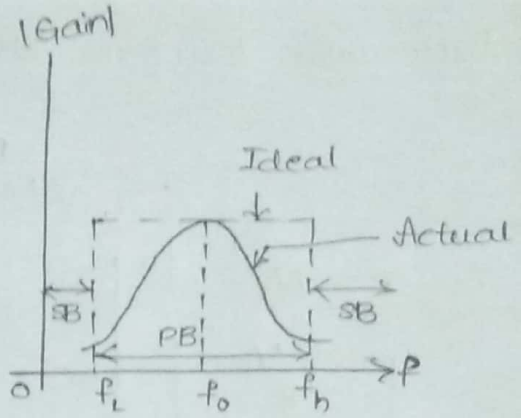
2) High pass filter:- The frequency response of HPF is

the passband allows the frequencies greater than f_L. stop band blocks the frequencies below f_L.



3) Band pass filter (BPF):-

A BPF has PB between f_L and f_h where $f_h > f_L$ and has 2 SB's i.e., $f > f_h$ and $0 < f < f_L$.

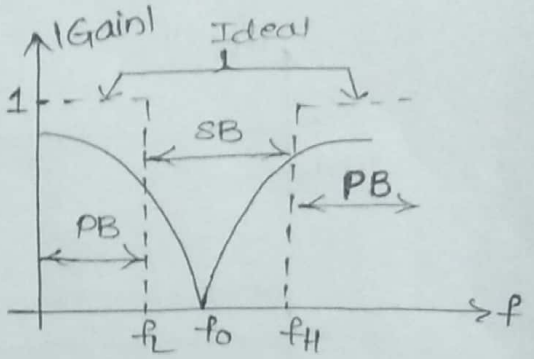


fig; Frequency Response of BPF.

4) Band stop filter (BSF):-

A BSF has SB between f_L and f_H where $f_H > f_L$ and has 2 PB's i.e., $f > f_H$; $0 < f < f_L$.

It is also called as Band Reject (or) Band elimination filter.



fig;-frequency response of BSF.

Butterworth Approximation:- The filter in which denominator polynomial of its transfer function is a butterworth polynomial is called a Butterworth filter. The Butterworth polynomials of various orders are given in the table.

n	polynomial equation
1	$S+1$
2	$S^2+\sqrt{2}S+1$
3	$(S^2+S+1)(S+1)$
4	$(S^2+0.76536S+1)(S^2+1.84775S+1)$
5	$(S+1)(S^2+0.618S+1)(S^2+1.618S+1)$

first order Butterworth low pass filter :-

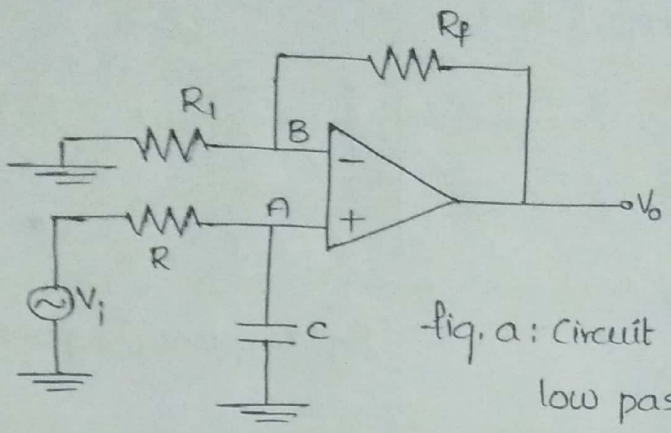


fig. a : Circuit diagram of first order low pass butterworth filter.

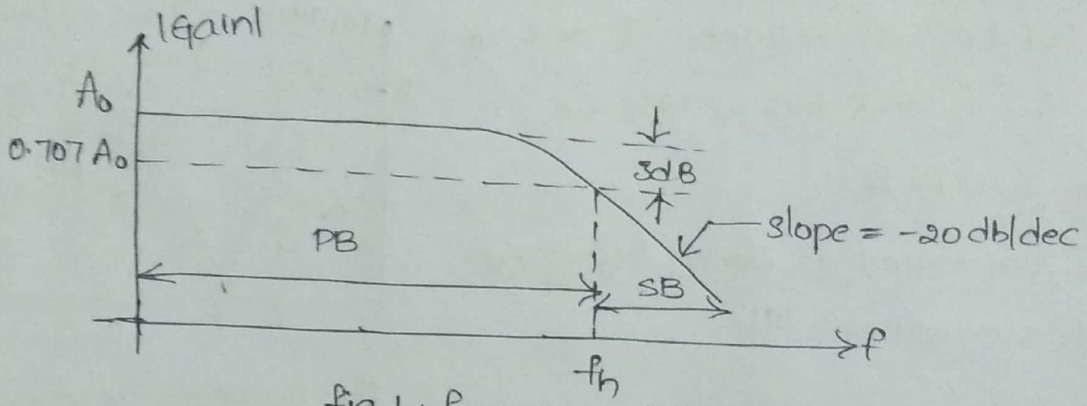


fig. b: frequency response.

→ The first order low pass butterworth filter is realised by RC circuit used along with op-amp, used in the non-inverting configuration.

→ It is also called one pole low pass Butterworth filter.

→ R_1 and R_f divide the gain of the filter in the pass band.

Circuit Analysis :-

Apply the potential divider rule at node A, which is the voltage across capacitor, C is given by (in s-domain),

$$V_A(S) = \frac{(1/sC)}{R + \frac{1}{sC}} \; V_i(S)$$

$$\frac{V_A(S)}{V_i(S)} = \frac{(1/sC)}{R + \frac{1}{sC}}$$

$$= \frac{1}{1 + SRC} \longrightarrow (1)$$

As the op-amp is in non-inverting configuration,

we know that $\frac{V_o(S)}{V_f(S)} = A_0 = 1 + \frac{R_f}{R_1} \longrightarrow (2)$

where A_0 is closed loop gain of op-amp

(or) gain of filter in pass band.

The overall transfer function from equations (1) and (2), we get

$$H(S) = \frac{V_o(S)}{V_i(S)} = \frac{V_o(S)}{V_A(S)} \cdot \frac{V_A(S)}{V_i(S)}$$

$$= A_0 \cdot \frac{1}{1+SRC}$$

$$= \frac{A_0}{1+SRC}$$

put $S = j\omega$

$$H(j\omega) = H(j2\pi f) = \frac{A_0}{1+j2\pi f RC}$$

where f_h = Upper cut off frequency $= \frac{1}{2\pi RC}$

$$\therefore \frac{V_o}{V_{in}} = \frac{A_0}{1+j(f/f_h)}$$

The gain and phase angle equations of the LPF can be obtained by converting above equation into its equivalent polar form as,

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

where $\left|\frac{V_o}{V_{in}}\right| = \frac{A_0}{\sqrt{1+(f/f_h)^2}} \longrightarrow (3)$

$$\phi = -\tan^{-1}(f/f_h) \longrightarrow (4)$$

ϕ is phase angle in degrees.

from eq.(3),

(i) At very low frequencies, $f < f_h$

$$\frac{f}{f_h} << 1$$

$$\left|\frac{V_o}{V_{in}}\right| = A_0$$

(ii) At $f = f_h$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_0}{\sqrt{2}} = 0.707\, A_0$$

(iii) At $f > f_h$, $\frac{f}{f_h} >> 1 \Rightarrow \left|\frac{V_o}{V_{in}}\right| < A_o$

→ Thus, LPF has a constant gain, A_o from $0Hz$ to f_h and $f = f_h$, the gain is $0.707 A_o$. After f_h, the gain decreases with a constant rate with increase in frequency.

→ The frequency f_h is called cut-off frequency because the gain of filter at this frequency is down by 3 decible ($= 20 \log 0.707$) from A_o

→ The cut-off frequency is also called as -3db frequency (or) break frequency (or) corner frequency.

Design steps:- The design steps for 1st low pass butterworth filter are

1. Choose cut-off frequency, f_h.
2. choose C value between 0.001μF to 1μF
3. Now, $f_h = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi f_h C}$
4. finally, select the values of R_1 and R_f dependent on the pass band gain of using,

$$A_o = 1 + \frac{R_f}{R_1}$$

Frequency Scaling:- Once the filter is designed, sometimes, it is necessary to change the value of cut-off frequency, f_h

→ The method used to change the original cut-off frequency, f_h to a new cut-off frequency, f_{h_1} is called as frequency scaling.

→ To achieve such a frequency scaling, the standard value capacitor, C is selected first.

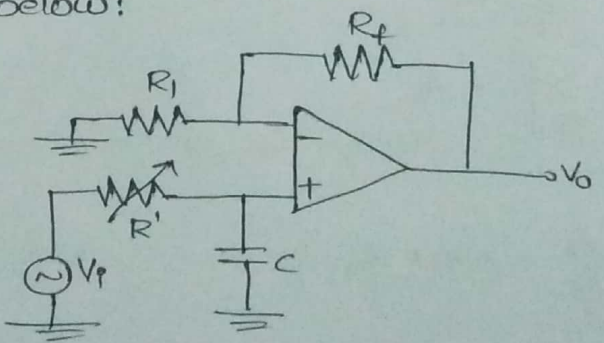
→ The required cut off frequency can be achieved by calculating the resistance, R value. To achieve frequency scaling, a potentiometer is used which is shown below:

New value of R' is

$$R' = R\left(\frac{f_c}{f_c'}\right)$$

f_c = original cut off frequency

f_c' = new cut off frequency.



→ The resistance, R is generally a potentiometer with which required cut-off frequency, f_h can be adjusted and changed later on if required.

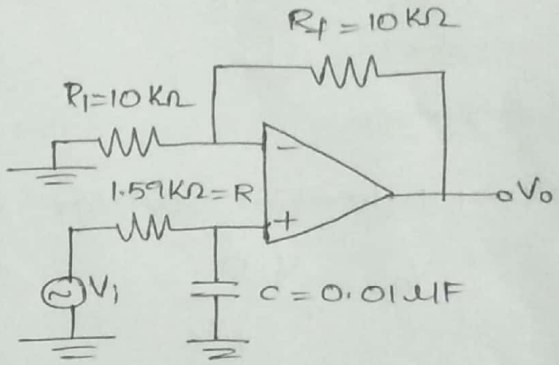
problem:-

1) Design a low pass filter at a cut-off frequency of 1KHz with a pass band gain of 2.

Sol:- Given cut-off frequency, $f_h = 1KHz$

PB gain $(A_0) = 2$

Design steps:-



1. $f_H = 1KHz$
2. choose $C = 0.01\mu F$
3. find R: $R = \frac{1}{2\pi f_h C}$

$$R = \frac{1}{2\pi \times 10^3 \times 0.01 \times 10^{-6}}$$

$$\boxed{R = 15.9\ K\Omega}$$

4. Select the values of R_f and R_1

$$2 = 1 + \frac{R_f}{R_1}$$

$$\frac{R_f}{R_1} = 1 \Rightarrow \boxed{R_f = R_1 = 10K\Omega}$$

2) Using frequency scaling technique, convert 1KHz cut off frequency of LPF is above example to a cut-off frequency of 1.6KHz.

Sol:- To change the cut off frequency from 1KHz to 1.6KHz.

New R value can be calculated by multiplying 15.9KHz resistor by original cut off frequency, f_c / New cut off frequency, f_c'.

$$\therefore \text{New } R = 15.9K \times \frac{f_c}{f_c'}$$

$$R = 15.9 \times \frac{1K}{1.6K}$$

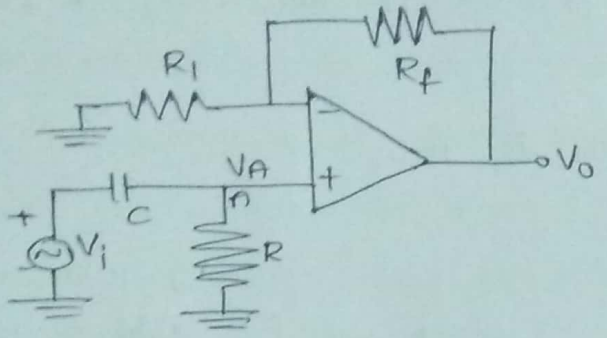
$$R = 9.94K\Omega$$

So, a potentiometer, R' of value $10K\Omega$ is used.

(ii) At $f > f_L$

First order High pass Butterworth filter :- High pass filters are often formed simply by interchanging frequency determining resistor and capacitor, in low pass filter.

Circuit diagram :-



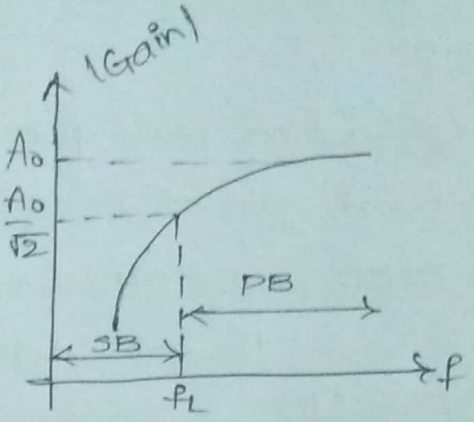


fig: frequency response

Circuit Analysis :-

Apply potential divider rule at A, we get

$$V_A = \frac{V_i \cdot R}{R - jX_C}$$

where $-jX_C = \frac{1}{2\pi f C j}$

$$V_A = \frac{V_i R}{R + \frac{1}{j2\pi f C}} \Rightarrow V_A = \frac{jV_i 2\pi f C}{1 + j2\pi f C}$$

$$\frac{V_A}{V_i} = \frac{j2\pi f C}{1 + j2\pi f C} \longrightarrow (1)$$

for non-inverting op-amp, w.k.t,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_A$$

where $A_o = 1 + \frac{R_f}{R_1}$ = pass band gain of filter

$$V_o = A_o V_A \longrightarrow (2)$$

Substitute the value of V_A in eq.(2), we get

$$V_o = \frac{A_o \cdot V_i \cdot j2\pi f C}{1 + j2\pi f RC}$$

$$\frac{V_o}{V_i} = \frac{A_o \cdot j2\pi f C}{1 + j2\pi f RC} \longrightarrow (3)$$

let $f_L = \frac{1}{2\pi RC}$ = lower cut off frequency.

from (3)., $\frac{V_o}{V_i} = \frac{A_0 \cdot j(f/f_L)}{1+j(f/f_L)}$

The magnitude of the voltage gain is $\left|\frac{V_o}{V_{in}}\right| = \frac{A_0(f/f_L)}{\sqrt{1+(f/f_L)^2}}$

→ Since, high pass filters are formed from low pass filters simply by interchanging resistor, R and capacitor, C. Therefore the design and frequency scaling procedure of LPF's are also applicable for HPF's.

Problem:-

i) Draw a HPF of a cut-off frequency 1KHz with a pass band gain of 2.

ii) Plot the frequency response for part (i).

Sol:- i) Design steps

1. choose $f_L = 1KHz$
2. choose $C = 0.01\mu f$
3. find R., $R = \frac{1}{2\pi f_L C}$

$$R = \frac{1}{2\pi \times 10^3 \times 0.01\mu} = 15.9\ k\Omega$$

4. To find R_1 and R_f such that $A_0 = 1 + \frac{R_f}{R_1}$

$$2 = 1 + \frac{R_f}{R_1}$$

$$R_f = R_1$$

choose $R_1 = 10K\Omega$

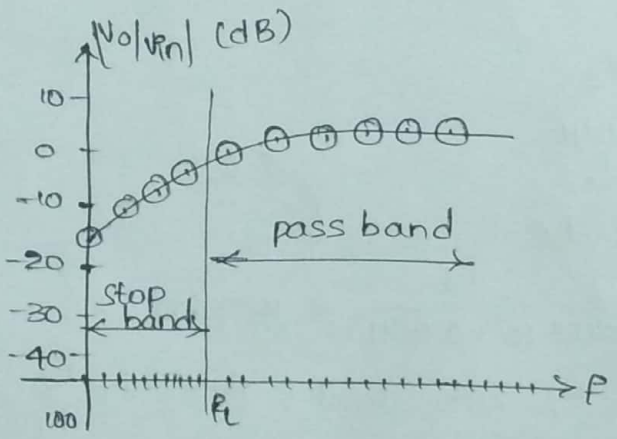
$\Rightarrow R_f = 10K\Omega$

ii) The frequency response plot can be obtained by substituting the input frequency values from 100Hz to 100KHz in the magnitude of the voltage gain equation and it is given by.,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_0(f/f_L)}{\sqrt{1+(f/f_L)^2}}$$

where $A_0 = 2$; $f = 1KHz$.

Frequency, f(Hz)	Gain magnitude $\left\|\frac{V_o}{V_{in}}\right\|$	Magnitude (dB) $= 20 \log \left\|V_o/V_{in}\right\|$
100	0.2	-14.02
200	0.39	-8.13
400	0.74	-2.58
700	1.15	1.19
1K	1.41	3.01
3K	1.8	5.56
7K	1.98	5.93
10K	1.99	5.98
30K	2	6.02
100K	2	6.02



Second order Butterworth low pass filter:-

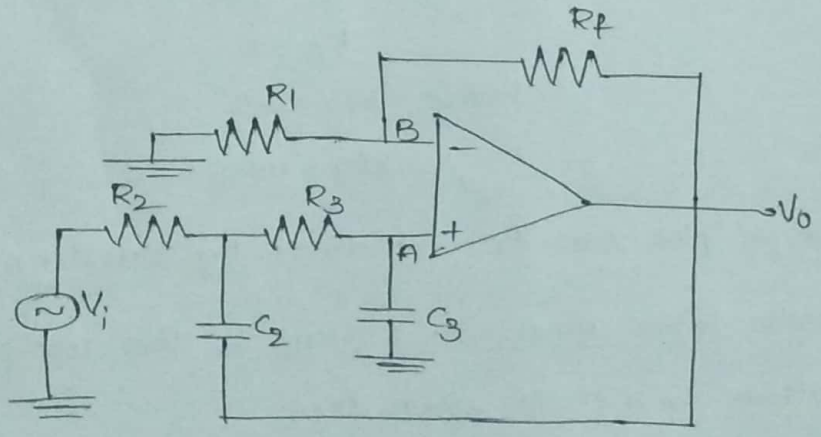


fig: Circuit diagram of second order low pass filter (Butterworth)

Band pass filter:- A BPF has a pass band between 2 cut off frequencies f_L and f_H such that $f_H > f_L$. Any input frequency outside the passband is attenuated.

→ There are two types of BPF's which are classified as per the figure of merit (or) Quality factor, Q.

i) Narrow BPF ($Q > 10$)

ii) Wide BPF ($Q < 10$)

→ The relation between Q and bandwidth is given as, $Q = \frac{f_c}{BW}$

$$Q = \frac{f_c}{f_H - f_L}$$

and $f_c = \sqrt{f_H \cdot f_L}$

where f_c = cut-off frequency

f_H = Upper cut off frequency

f_L = lower cut off frequency

→ If the Quality factor increases, then the BW gets decreases.

i) Narrow BPF:- NBPF:- The circuit of NBPF has two feedback paths and the op-amp is used in inverting mode of operation.

Circuit Analysis:-

For fig(a), Take nodal analysis at point A.,

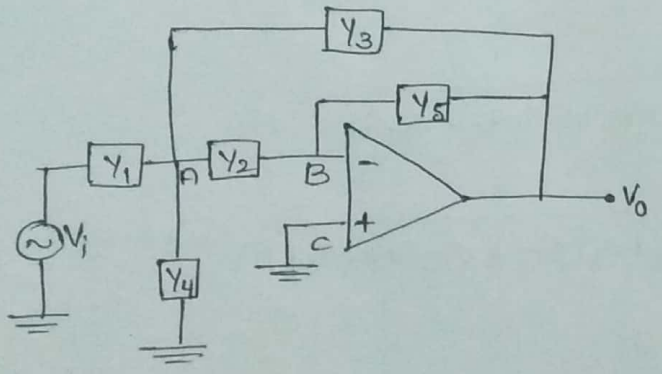


Fig.(a): Band-pass configuration

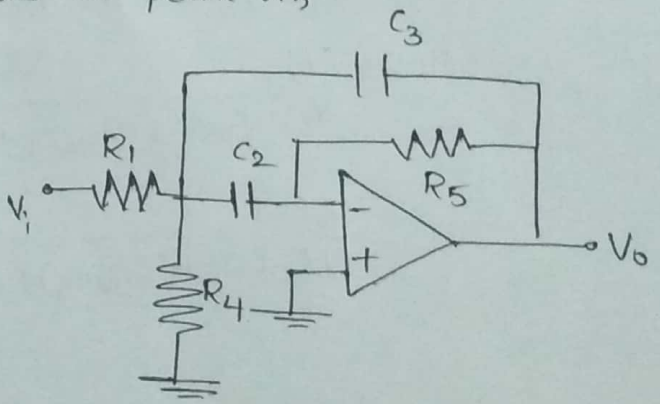


fig.(b): Second order BPF

$$(V_A - V_i)Y_1 + V_A Y_4 + (V_A - V_o)Y_3 + (V_A - V_B)Y_2 = 0$$

$$V_d = 0 \Longrightarrow V_B = V_C$$

$$V_B = 0.$$

$$V_A(Y_1+Y_2+Y_3+Y_4) = V_i Y_1 + V_o Y_3$$

$$V_A = \frac{V_i Y_1 + V_o Y_3}{Y_1+Y_2+Y_3+Y_4} \longrightarrow (1)$$

Take node equation at node 'B',,

$$(V_B - V_A)\, Y_2 + (V_B - V_o)\, Y_5 = 0$$

$$-V_A Y_2 - V_o Y_5 = 0$$

$$V_A = -\frac{V_o Y_5}{Y_2} \longrightarrow (2)$$

$$(1) = (2)$$

$$\frac{V_i Y_1 + V_o Y_3}{Y_1+Y_2+Y_3+Y_4} = \frac{-V_o Y_5}{Y_2}$$

$$-V_o\left[(Y_1+Y_2+Y_3+Y_4)\, Y_5 + Y_3 Y_2\right] = V_i Y_1 Y_2$$

$$\frac{V_o}{V_i} = \frac{-Y_1 Y_2}{Y_1Y_5 + Y_2Y_3 + Y_2Y_5 + Y_3Y_5 + Y_4Y_5} \longrightarrow (3)$$

This circuit can be band pass filter, put $Y_1 = G_1$; $Y_2 = SC_2$; $Y_3 = SC_3$;

$Y_4 = G_4$; $Y_5 = G_5$.

Then the transfer function becomes,

$$H(S) = \frac{V_o}{V_i} = \frac{-SG_1C_2}{G_1G_5 + S^2C_2C_3 + SC_2G_5 + SC_3G_5 + G_4G_5}$$

$$\frac{V_o(S)}{V_i(S)} = \frac{-SG_1C_2}{S^2(C_2C_3) + S(C_2+C_3)G_5 + G_5(G_1+G_4)}$$

$$= \frac{-G_1}{SC_3 + \frac{G_5(C_2+C_3)}{C_2} + \frac{(G_1+G_4)G_5}{SC_2}} \longrightarrow (4)$$

→ The transfer function of eq.(4) is equivalent to the gain expression of a parallel RLC circuit as shown in below figure (a).

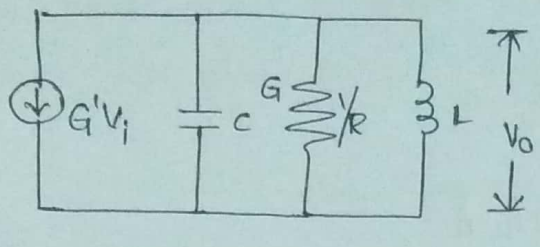


fig.(a). parallel RLC circuit

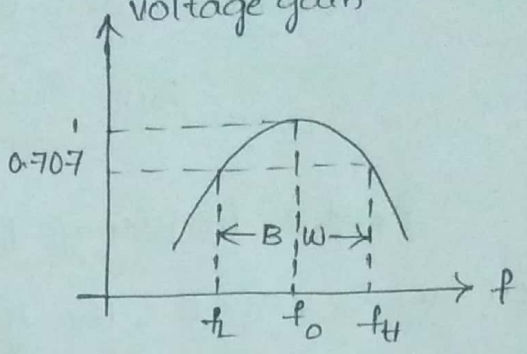


fig.(b): Band pass characteristics.

→ The gain expression of fig(a) is given as,

$$\frac{V_o(s)}{V_i(s)} = \frac{-G'}{Y} = \frac{-G'}{sC+G+1/sL} \longrightarrow (5)$$

comparing the gain expression (4) and (5), we get

$$G' = G_1$$

$$L = \frac{C_2}{G_5(G_1+G_4)}$$

$$G = \frac{G_5(C_2+C_3)}{C_2}$$

$$C = C_3$$

→ At resonance, the parallel RLC circuit has unity power factor i.e, imaginary part is zero. This gives the resonant frequency ω_0 as

$$\omega_0^2 = \frac{1}{LC} = \frac{G_5(G_1+G_4)}{C_2C_3}$$

$$\omega_0 = \sqrt{\frac{G_5(G_1+G_4)}{C_2C_3}}$$

→ The gain at resonance is

$$\left.\frac{V_o}{V_i}\right|_{\omega=\omega_0} = \frac{-G'}{G} = \frac{-G_1}{G} = \frac{-G_1(G_5)C_2}{C_2+C_3}$$

→ The Q-factor at resonance is

$$Q_0 = \omega_0 RC = \frac{\omega_0 C}{G} = \frac{\omega_0 C_2C_3}{(C_2+C_3)G_5}$$

→ The Bandwidth is given by

$$BW = f_H - f_L = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi R \omega_0 C} = \frac{G}{2\pi C}$$

$$BW = \frac{G_5(C_2+C_3)}{2\pi C_2 C_3}$$

Centre frequency, $f_0 = \sqrt{f_H f_L}$

→ Now for $C_2 = C_3 = C$, the gain at resonant frequency is given as,

$$\left.\frac{V_0}{V_i}\right|_{\omega=\omega_0} = \frac{-R_5}{+2R_1} = -A_0$$

$$\omega_0 = \frac{\sqrt{G_5(G_1+G_4)}}{C}$$

$$BW = \frac{G_5}{\pi C} = \frac{1}{\pi R_5 \cdot C}$$

→ The standard transfer function of a BPF is obtained as.,

$$H(s) = \frac{-A_0(\omega_0/Q)s}{s^2+(\omega_0/Q)s+\omega_0^2} = \frac{-A_0\alpha\cdot\omega_0 s}{s^2+\alpha\omega_0 s+\omega_0^2}$$

where the damping factor, $\alpha = \frac{1}{Q}$.

→ Gain in dB, $20\log|H(s)| = 20\log\left|\frac{A_0\alpha\cdot\omega_0 s}{s^2+\alpha\omega_0 s+\omega_0^2}\right|$

→ In NBPF, the new value of resistance is $R_4' = R_4(f_c/f_c')^2$

where f_c = original cut off frequency

f_c' = New cut off frequency.

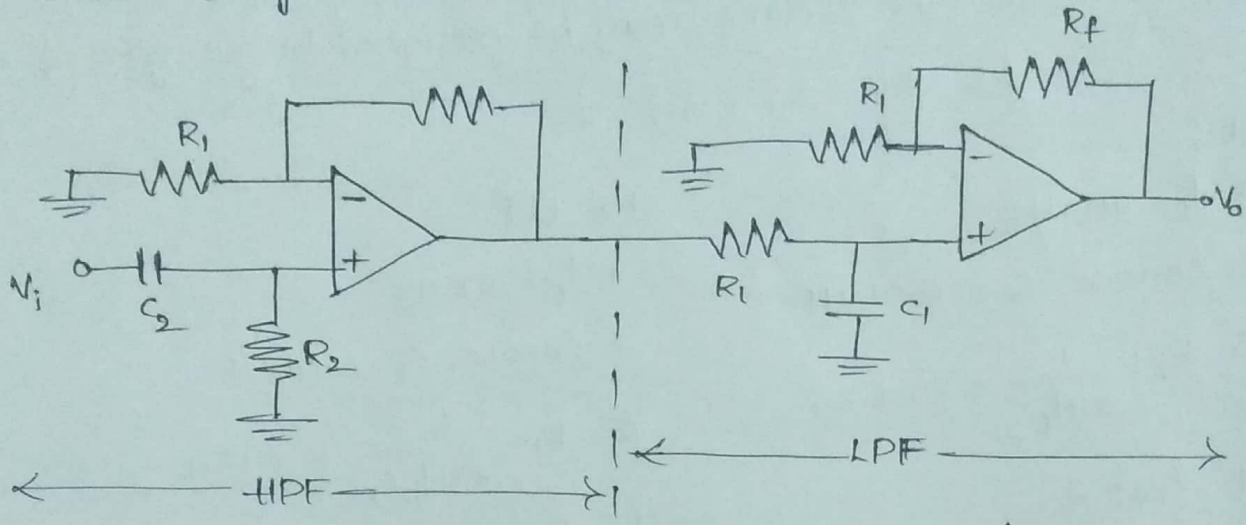
Design steps for NBPF:

→ $C_2 = C_3 = C$

→ $R_1 = \frac{Q}{2\pi f_0 C A_0}$ → $R_3 = \frac{Q}{\pi f_0 C}$

→ $R_4 = \frac{Q}{2\pi f_0 C(2Q^2 - A_0)}$

ii) Wide band pass filter:- A WBPF can be formed by cascading a HPF and LPF section. If the HPF and LPF are of 1st order then the band pass filter will have a roll-off rate of -20db/decade The circuit diagram of 1st order WBPF is shown below;



for HPF, the magnitude of gain is $|H_{HP}| = \frac{A_{01}}{\sqrt{1+(f_L/f)^2}} \rightarrow (1)$

Similarly, for low pass filter section, the magnitude of gain is,

$$|H_{LP}| = \frac{A_{02}}{\sqrt{1+(f/f_h)^2}} \rightarrow (2)$$

→ The magnitude of voltage gain of the WBPF is the product of LPF and HPF is

$$\left|\frac{V_o}{V_i}\right| = \frac{A_0}{\sqrt{(1+(f/f_h)^2)(1+(f_L/f)^2)}}$$

(or)

$$= \frac{A_0(f/f_L)}{\sqrt{(1+(f/f_L)^2)(1+(f/f_h)^2)}} \rightarrow (3)$$

Similarly, for 2nd order WBPF, 2nd HPF & 2nd LPF are to be cascaded.

problem:- Design a WBPF having $f_L = 400Hz$; $f_H = 2KHz$; pass band gain of 4. find the value of Q of the filter.

Sol:- Given pass band filter, $A_0 = 4$

So, for LPF and HPF sections may be designed to give gain of 2.

i.e., $A_{01} = 2$; $A_{02} = 2$.

For HPF;

1. $f_L = 400Hz$
2. Choose $C_2 = 0.01\mu F$
3. $R_2 = \frac{1}{2\pi f_L C_2} = 39.8\ K\Omega$
4. $A_{01} = 2$

$1 + \frac{R_f}{R_1} = 2$

$R_f = R_1 = 10K\Omega$

For LPF.,

1. $f_h = 2KHz$
2. Choose $C_1 = 0.01\mu F$
3. $R_1 = \frac{1}{2\pi f_h C_1} = 7.9K\Omega$
4. $A_{02} = 2$

$1 + \frac{R_f}{R_1} = 2$

$R_f = R_1 = 10K\Omega$

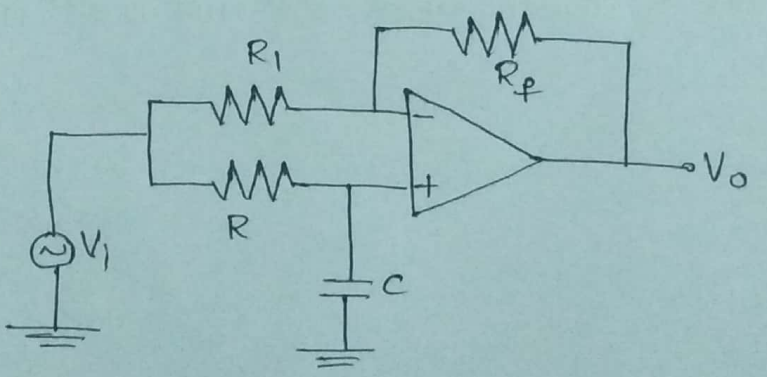
Now, $f_0 = \sqrt{f_H \cdot f_L} = \sqrt{2K \times 400} = 894.4\ Hz$

Quality factor, $Q = \frac{f_0}{BW} = \frac{f_0}{f_H - f_L} = \frac{894.4}{(2K-400)} = 0.56$ ($\because Q < 10$).

All pass filter:- (APF) (phase corrector).

The APF allows all frequencies of the input signal without any attenuation and provides phase for different frequencies of the signal.

These All pass filters are also called as delay equalizer and phase correctors.



Circuit analysis:-

Using super position theorem, the o/p voltage expression is

$$V_o = V_{o1} + V_{o2}.$$

V_{o1} ⇒ o/p voltage when V_{in} is applied at -ve terminal.,

$$V_{o1} = -\frac{R_f}{R_1} \cdot V_i \longrightarrow (1)$$

V_{o2} ⇒ o/p voltage when V_{in} is applied at +ve terminal.,

$$V_{o2} = \left(1 + \frac{R_f}{R_1}\right) V_A \longrightarrow (2)$$

$$V_o = \left(\frac{-R_f}{R_1}\right) V_i + \left(1 + \frac{R_f}{R_1}\right) V_A \longrightarrow (3)$$

choose $R_1 = R_f$

Apply the potential divider rule to calculate the value of V_A,

$$V_A = \frac{V_i(1/sC)}{R + 1/sC} = \frac{V_i}{1+SRC}$$

Substitute V_A in (3).,

$$V_o = -V_i + \frac{2V_i}{1+SRC}$$

$$V_o = V_i\left[\frac{-1-SRC+2}{1+SRC}\right]$$

$$\frac{V_o}{V_i} = \frac{1-SRC}{1+SRC}$$

put $S = j\omega = j2\pi f$

$$\frac{V_o}{V_i} = \frac{1-j2\pi fRC}{1+j2\pi fRC}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{1-j2\pi fRC}{1+j2\pi fRC} = 1$$

$$\varphi = \tan^{-1}(-2\pi fRC) - \tan^{-1}(2\pi fRC)$$

$$\varphi = -2\tan^{-1}(2\pi fRC)$$

Band Reject filter (BRF):- A BRF is also called as Band stop (or) Band elimination filter. A BRF has two pass bands and one stop band. In this, $f_l > f_h$ there are two types of BRF's which are classified as per the figure of merit (or) Quality factor

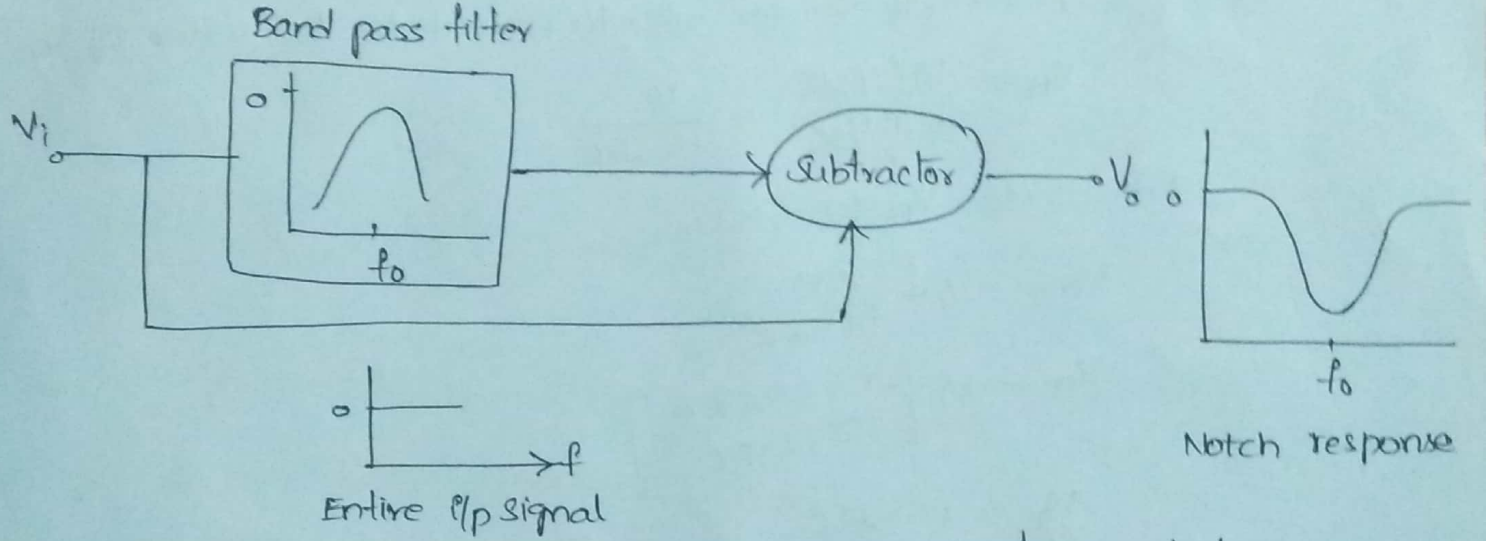
i) Narrow BRF ($Q > 10$)

ii) Wide BRF ($Q < 10$)

i) Narow BPF:- The narrow band reject filter is commonly called a notch filter and is useful for the rejection of a single frequency

→ There are several ways to make notch filter. One simple technique is to subtract the band pass filter output from its input

→ The notch filter block diagram is shown below:



→ The practical notch filter block diagram is shown below.

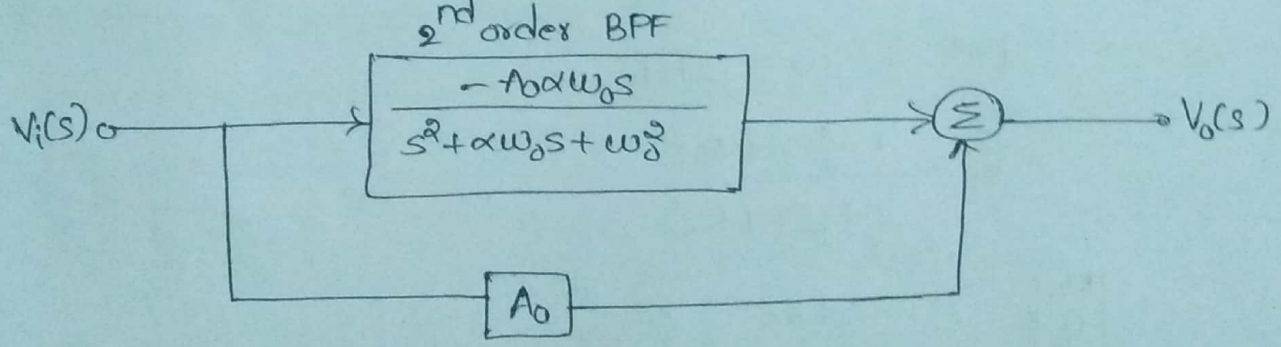


Fig.(b). Block diagram of practical Notch filter.

→ In practical, the gain of o/p of BPF is negative. So, we are using a summer instead of a subtractor.

→ One input to the summer is output of 2nd order BPF and the other i/p is A_0V_i.

→ Therefore, the o/p of the circuit in s-domain is,

$$V_o(s) = A_0V_i(s) - \frac{A_0\alpha\omega_0 s}{s^2+\alpha\omega_0 s+\omega_0^2}$$

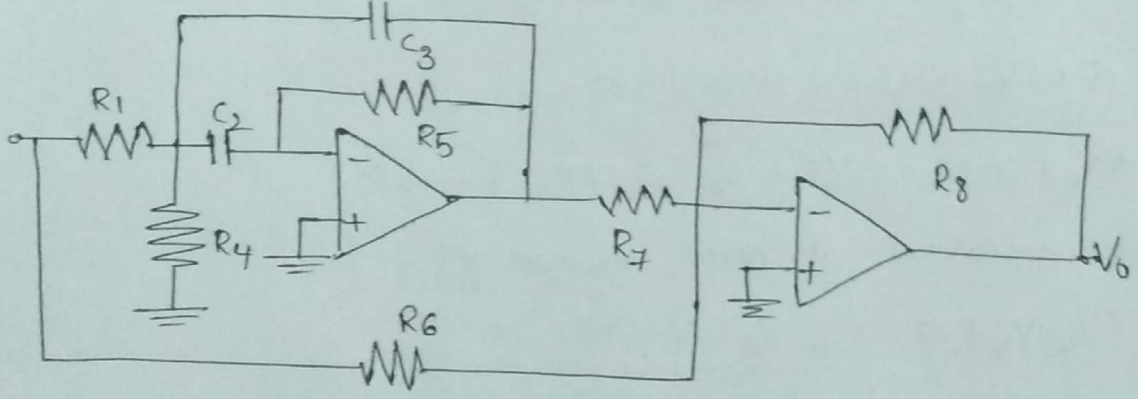
$$\frac{V_o(s)}{V_i(s)} = A_0\left(1 - \frac{\alpha\omega_0 s}{s^2+\alpha\omega_0 s+\omega_0^2}\right) = \frac{A_0(s^2+\omega^2)}{s^2+\omega_0 s\alpha+\omega_0^2}$$

$$\boxed{\frac{V_o(s)}{V_i(s)} = \frac{A_0(s^2+\omega^2)}{s^2+\alpha\omega_0 s+\omega_0^2}}$$

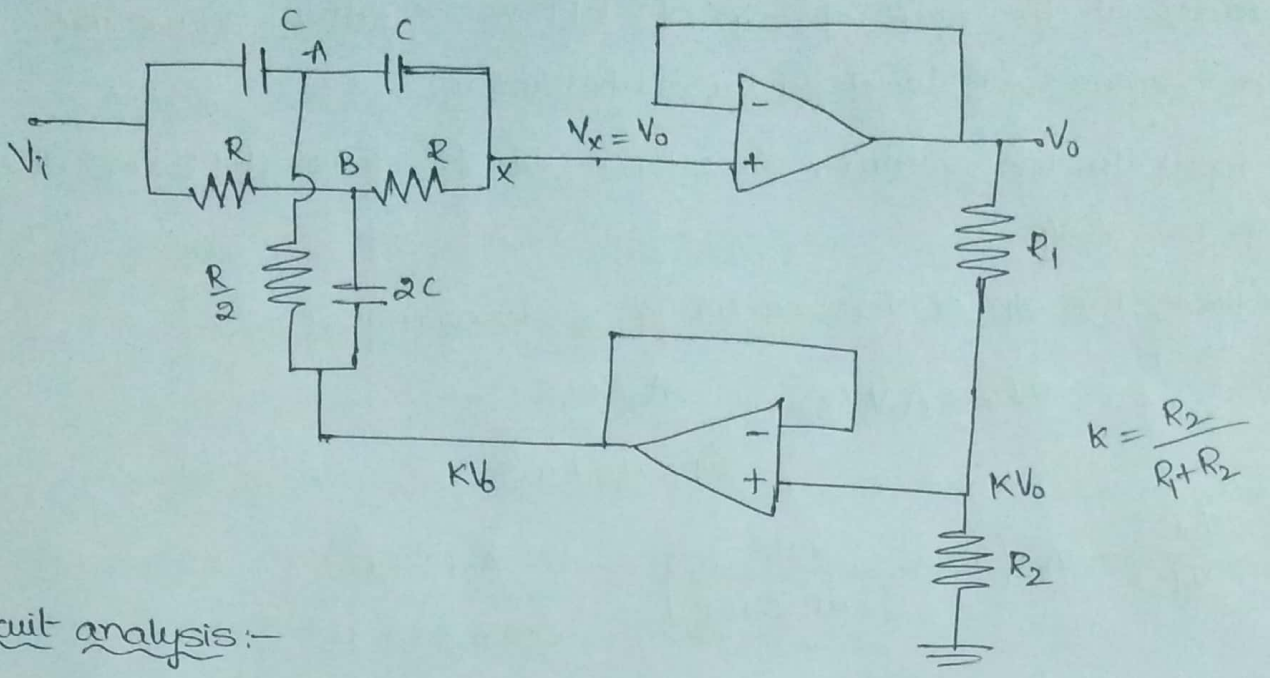
⇓

This is the standard transfer function for a 2nd order notch filter.

→ The circuit schematic is shown below:



* Another commonly used notch filter in the twin-T network as shown in below figure,



Circuit analysis :-

Take nodal equation at node A, we get

$$(V_A - V_i)\,sC + (V_A - V_o)\,sC + (V_A - KV_o)\,2G = 0$$

$$2V_A(sC+G) = V_i sC + V_o(sC+2KG) \longrightarrow (1)$$

Take nodal analysis at node B, we get

$$(V_B - V_i)\,G + (V_B - KV_o)\,2sC + (V_B - V_o)\,G = 0$$

$$2V_B(sC+G) = V_i G + V_o(G+2KsC) \longrightarrow (2)$$

Take nodal equation at node x, we get

$$(V_o - V_B)\,G + (V_o - V_A)\,sC = 0$$

$$V_B G = V_o(G+sC) - V_A sC$$

$$V_B = \frac{V_o(G+sC) - V_A sC}{G} \longrightarrow (3)$$

Substitute the value of V_B in eq.(2), we get

$$2(sC+G)\left[\frac{V_o(G+sC) - V_A sC}{G}\right] = V_i G + V_o(G+2KsC) \longrightarrow (4)$$

from (1), $V_A = \dfrac{V_i \cdot sC + V_o(sC+2KG)}{2(G+sC)}$

From (4).,
$$\frac{2V_o(G+sC)^2}{G} - \frac{2V_A sC(sC+G)}{G} = V_i G + V_o[G+2KsC] \longrightarrow (5)$$

Substitute the value of V_A in eq.(5), we get

$$\frac{2V_o(G+sC)^2}{G} - \frac{2sC(sC+G)}{G} \times \frac{V_i \cdot sC + V_o(sC+2KG)}{2(sC+G)} = V_i G + V_o(G+2KsC)$$

$$2V_o[G^2+s^2C^2+2GsC] - (V_i s^2C^2 + V_o s^2C^2 + 2sCKGV_o) = V_i G^2 + V_o G^2 + 2V_o KGsC.$$

$$2V_o G^2 + 2V_o s^2C^2 + 2\cdot 2V_o GsC - V_i s^2C^2 - V_o s^2C^2 - 2sCKV_o G = V_i G^2 + V_o G^2 + 2V_o KGsC$$

$$V_o G^2 + V_o s^2C^2 - 4V_o KGsC + 4V_o GsC = V_i(G^2+s^2C^2)$$

$$V_o[s^2C^2 + 4GsC(1-K) + G^2] = V_i[G^2+s^2C^2]$$

$$\frac{V_o}{V_i} = \frac{G^2+s^2C^2}{s^2C^2+G^2+4GsC(1-K)}$$

Transfer function,

$$H(s) = \frac{V_o}{V_i} = \frac{G^2+s^2C^2}{s^2C^2+G^2+4GsC(1-K)}$$

$$\boxed{H(s) = \frac{V_o}{V_i} = \frac{s^2+(G/C)^2}{s^2+(G/C)^2+4(1-K)\cdot s(G/C)}} \longrightarrow (6)$$

where $\omega_0 = G/C \Rightarrow f_0 = \frac{1}{2\pi RC}$

put $s = j\omega$ in eq.(6).,

$$H(j\omega) = \frac{\omega^2-\omega_0^2}{\omega^2-\omega_0^2-j4(1-K)\omega\omega_0}$$

→ At 3dB point, $|H(j\omega)| = \frac{1}{\sqrt{2}}$

$$\left|\frac{\omega^2-\omega_0^2}{\omega^2-\omega_0^2-j4(1-K)\omega\omega_0}\right| = \frac{1}{\sqrt{2}}$$

$$\frac{(\omega^2-\omega_0^2)}{\sqrt{(\omega^2-\omega_0^2)+(4(1-K)\omega\omega_0)^2}} = \frac{1}{\sqrt{2}}$$

$$(\omega^2-\omega_0^2)^2 + (4(1-K)\omega\omega_0)^2 = 2(\omega^2-\omega_0^2)^2$$

$$(\omega^2-\omega_0^2)^2 = (4(1-K)\omega\omega_0)^2$$

$$\omega^2-\omega_0^2 = \pm 4(1-K)\omega_0\omega \quad (\because \text{Take square root on both sides})$$

Now, $(\omega/\omega_0)^2 \pm 4(1-K)\omega/\omega_0 - 1 = 0$

Solve this quadratic equation, we get the upper and lower half power frequencies as,

$$f_h = f_0\left[\sqrt{1+4(1-K)^2} + 2(1-K)\right]$$

$$f_l = f_0\left[\sqrt{1+4(1-K)^2} - 2(1-K)\right]$$

Now, 3dB bandwidth,

$$BW = f_h - f_l = 4(1-K)f_0$$

Now $Q = \frac{f_0}{BW} = \frac{1}{4(1-K)}$

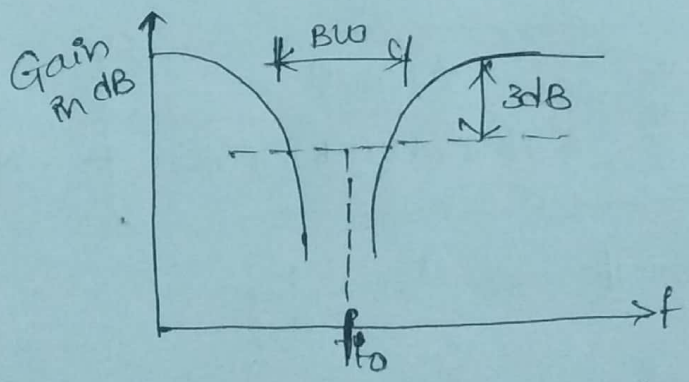
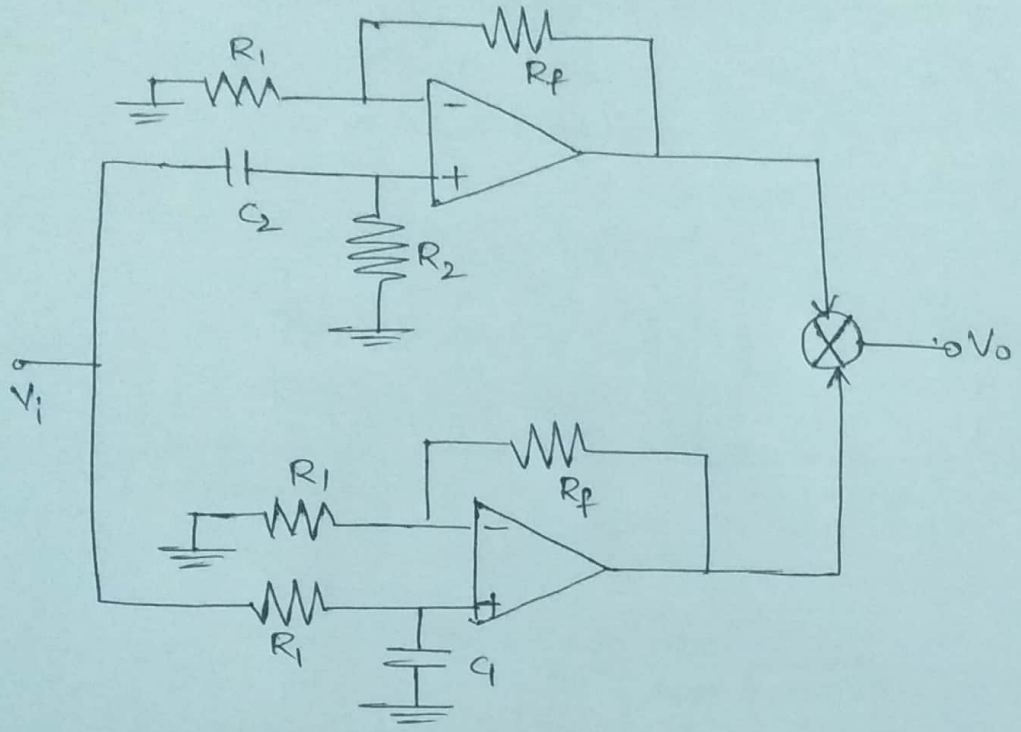


fig: frequency response of notch filter.

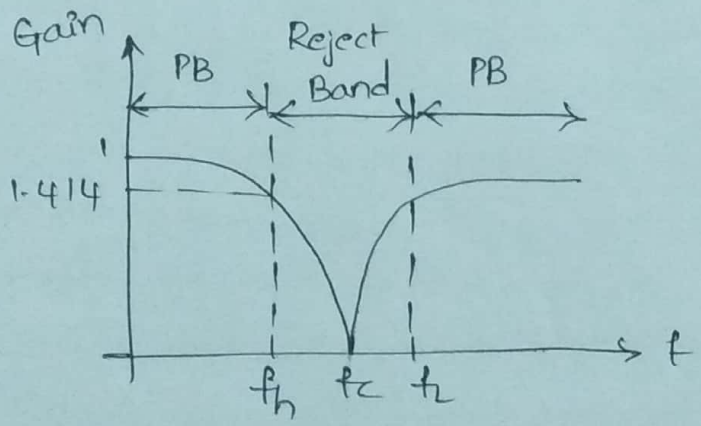
Wide Band Reject filter (WBRF): A WBRF can be made using a LPF, HPF and a summer. It is necessary that

i) the lower cut off frequency, f_l of the HPF should be much greater than the upper cut off frequency, f_h of the LPF.

ii) The pass band gain of LPF and HPF should be same.



→ The frequency response of a WBRF is shown below.



UNIT-V

555 Timer

555 Timer :- The 555 timer is a highly stable device for generating accurate time delay or oscillations. The Pin diagram for SE555/NE 555 is shown below.

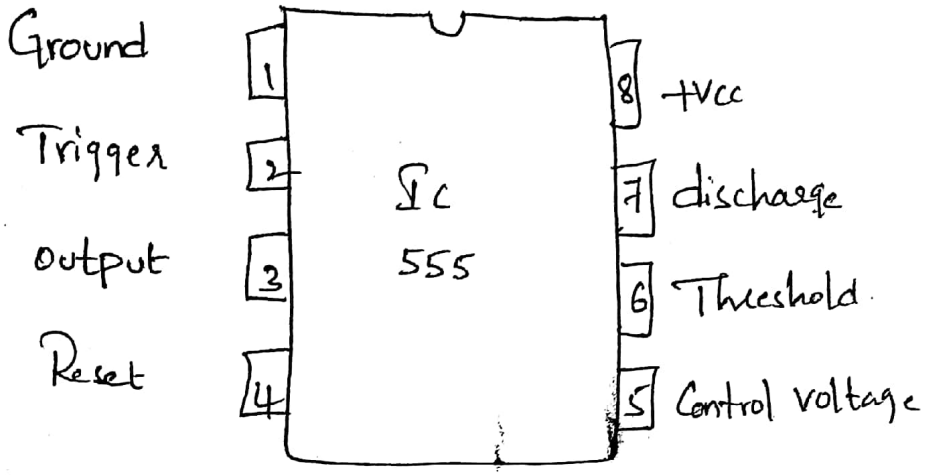


fig :- Pin diagram IC 555

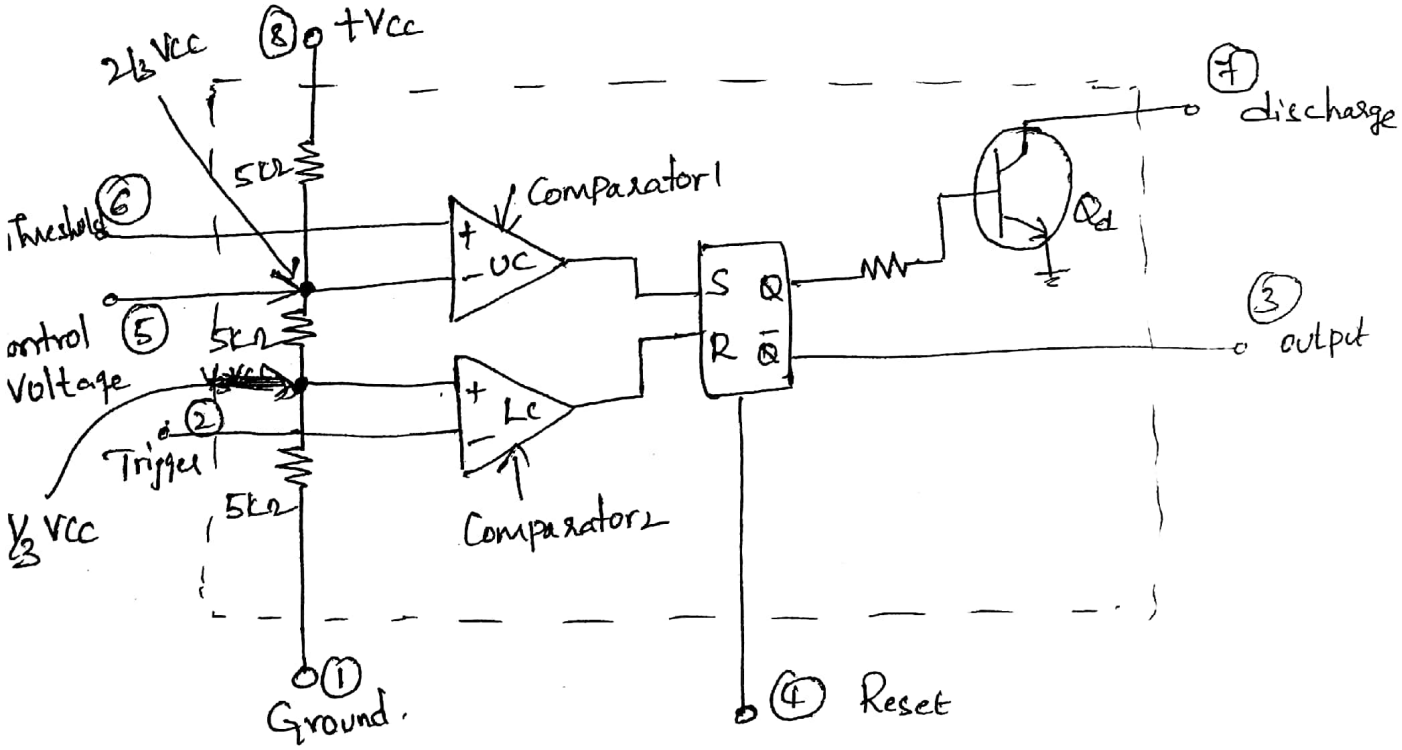


fig :- Block diagram of IC 555 timer.

Circuit description:- The IC 555 timer internally consists of Three 5 KΩ Resistors and this Three 5KΩ resistors acts as voltage divider Provide bias voltage of 2/3 of Vcc to the upper Comparator (UC) and 1/3 of Vcc to lower Comparator where Vcc is the supply voltage since these 2 voltages fix the necessary Comparator threshold voltage.

Circuit operation:-

In the stable state the o/p $\bar{Q}$ of the Controlled ff is high this makes the o/p low because of Power amplifier which is basically an inverter

→ when a -ve going trigger pulse is applied to pin 2, as the -ve edge of the trigger passes through 1/3 Vcc, the o/p of the lower Comparator becomes HIGH. and it sets the Control FF making Q=1 and $\bar{Q}$=0.

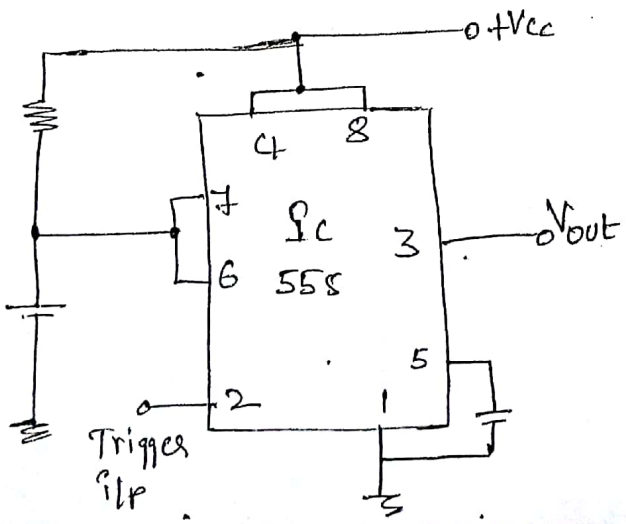
→ when the threshold voltage at pin6 exceeds 2/3 Vcc, the o/p of Upper Comparator (Comparator1) goes HIGH. This action resets the Control FF with Q=0 & $\bar{Q}$=1

→ The Reset i/p (Pin4) Provides a mechanism to reset the flip flop when this reset is not used it is returned to Vcc.

→ The transistor Q_2 serves as a Buffer to isolate the reset i/p from the flipflop and the transistor Q_1. The transistor Q_2 is driven by an internal reference voltage. Vref obtained from the supply voltage Vcc.

Monostable multivibrator:-

The IC 555 timer can be operated as a monostable multivibrator by Connecting an External resistor and a Capacitor.



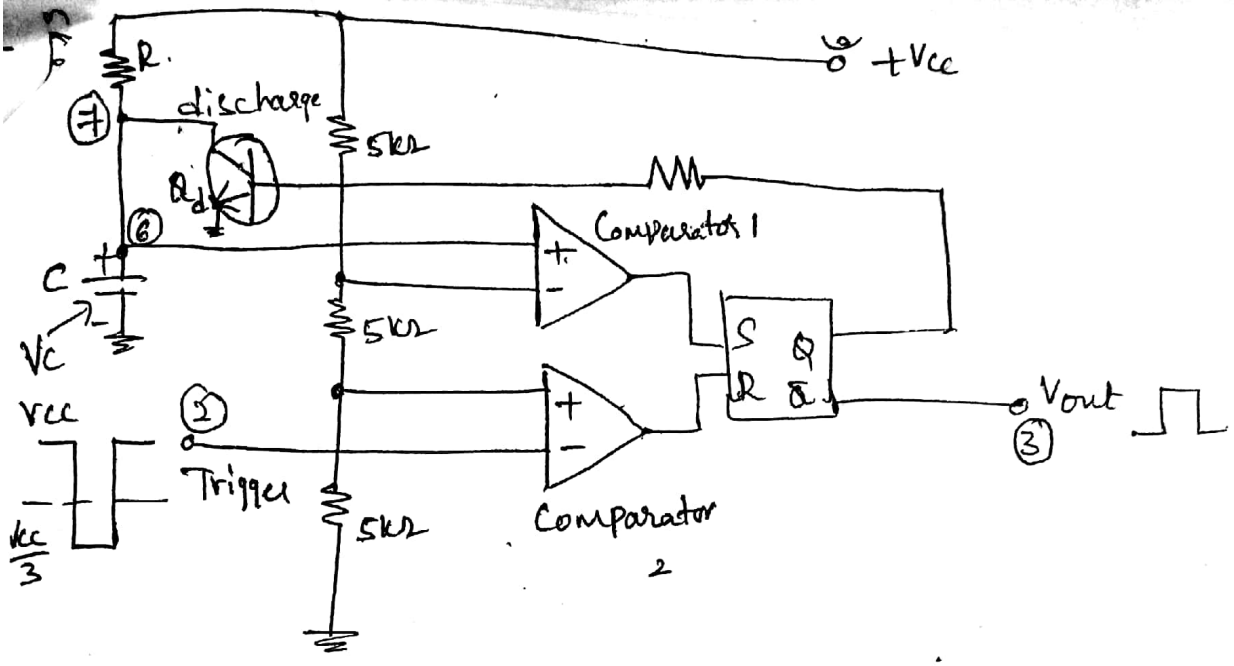


fig :- Monostable operation of 555.

As it has only one stable state, it is called one shot multivibrator

Circuit operation :-

→ The Flipflop is initially set i.e Q is high. This drives the transistor Q_d in Saturation. The Capacitor discharges Completely and voltage across it is nearly zero. The o/p at Pin 3 is low.

→ When a trigger i/p, a low going Pulse is applied, then Circuit state remains unchanged till trigger voltage is greater than $\frac{1}{3}V_{cc}$. When it becomes less than $\frac{1}{3}V_{cc}$, then Comparator 2 output goes high. Low Q makes the transistor Q_d off. Hence capacitor starts charging through resistance R.

→ The voltage across capacitor increases Exponentially. This voltage is nothing but the threshold voltage at Pin 6. When this voltage becomes more than $\frac{2}{3}V_{cc}$, then Comparator 1 output goes high. This sets the flipflop. i.e Q becomes high and $\bar{Q}$ low. This high Q drives the transistor Q_d in Saturation. Thus Capacitor C quickly discharges through Q_d

→ So it can be noted that Vout at Pin 3 is low at start, when trigger is less than $\frac{1}{3}V_{cc}$ it becomes high and when threshold is greater than $\frac{2}{3}V_{cc}$ again becomes low., till next Pulse occurs. So a rectangular wave is Produced at the output.

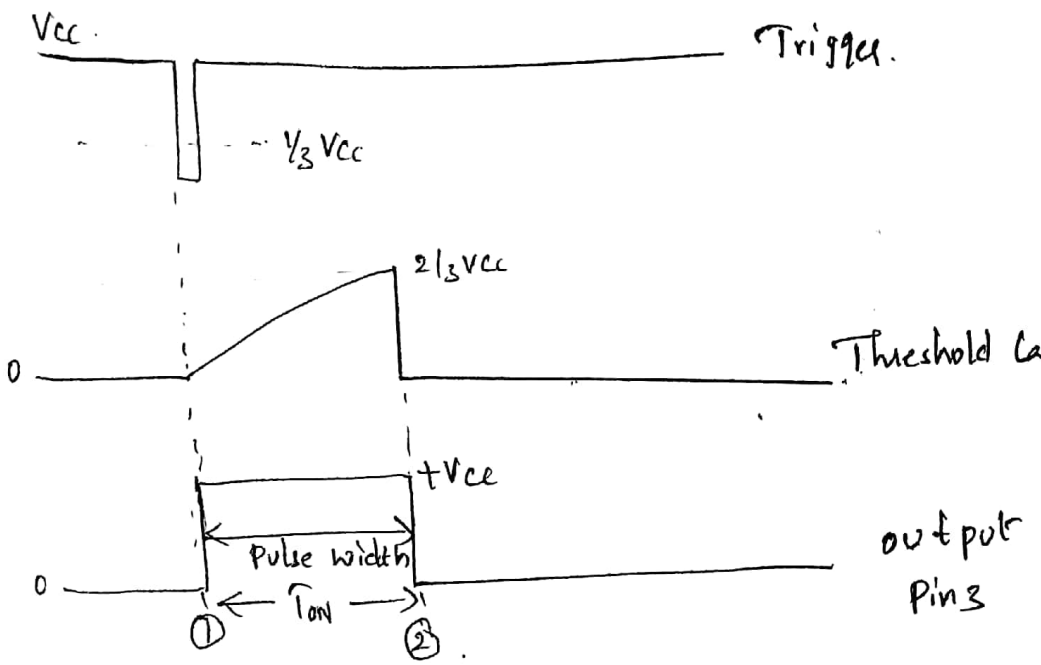


fig:- waveforms of monostable operation.

Derivation of Pulse width

The voltage across Capacitor increases exponentially and is given by

$$V_C = V_{cc}(1-e^{-t/Rc})$$

if $V_C = 2/3\ V_{CC}$

then $2/3\ V_{CC} = V_{cc}(1-e^{-t/Rc})$.

$$2/3 - 1 = -e^{-t/Rc}$$

$$\frac{1}{3} = e^{-t/Rc}$$

$$-\frac{t}{Rc} = -1.0986$$

$$t = +1.0986\ CR$$

$$t = 1.1\ RC$$

where C in farads, R is ohms, t in seconds.

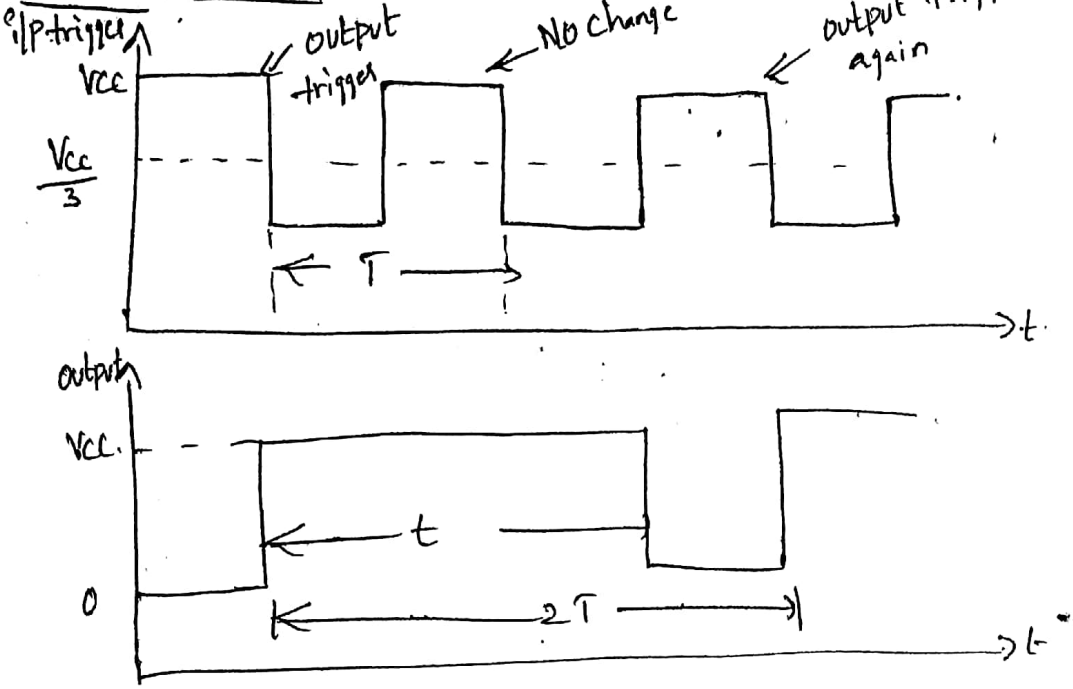
Thus, we can say that voltage across Capacitor will reach $2/3\ V_{CC}$, in approximately 1.1 times, time Constant i.e 1.1RC.

Thus the Pulse width denoted as w is given by

$$\boxed{W = 1.1RC}$$

...lications of Monostable multivibrator

Frequency divider :-



→ A Continuously triggered monostable ckt when trigger by a Square wave Generator can be used as a frequency divider if the timing interval is adjusted to be longer than the Period of the triggering Square wave i/p Signal.

→ The monostable multivibrator will be triggered by the 1st -ve going edge of the Square wave i/p but the o/p will remain HIGH for next -ve going edge of the Square wave i/p

→ The monoshot will however be triggered on the 3rd -ve going i/p depending on the choice of the time delay.

→ In this way the o/p can be made integral fraction of the frequency of the i/p triggering Square wave

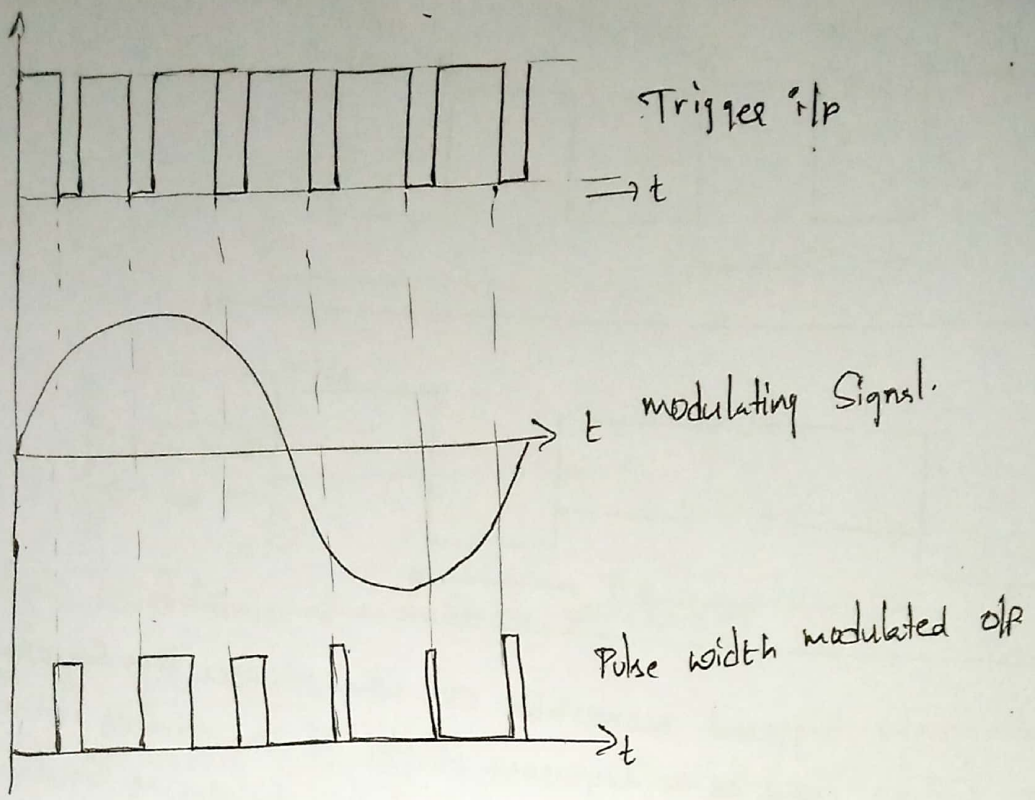
Pulse width Modulation

→ It is basically a monostable multivibrator with a modulating i/p Signal applied at the Control voltage input. Internally, the Control voltage is adjusted to the 2/3 Vcc.

→ Externally applied modulating Signal changes the Control voltage, and hence the upper Comparator.

→ As a result, time Period required to change the Capacitor upto

Threshold voltage changes, giving pulse width modulated signal at R



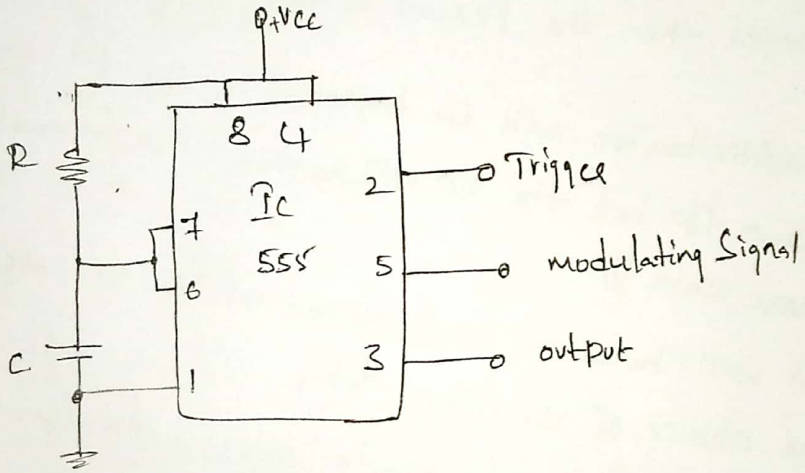


fig:- PWM

Linear Ramp Generator :-

→ When a Capacitor is Charged with a Constant Current Source then a linear Ramp is obtained. This Concept is Used as a linear Ramp generator

→ The ckt is Used to obtained Constant Current Ic Using transistor Q and diode D

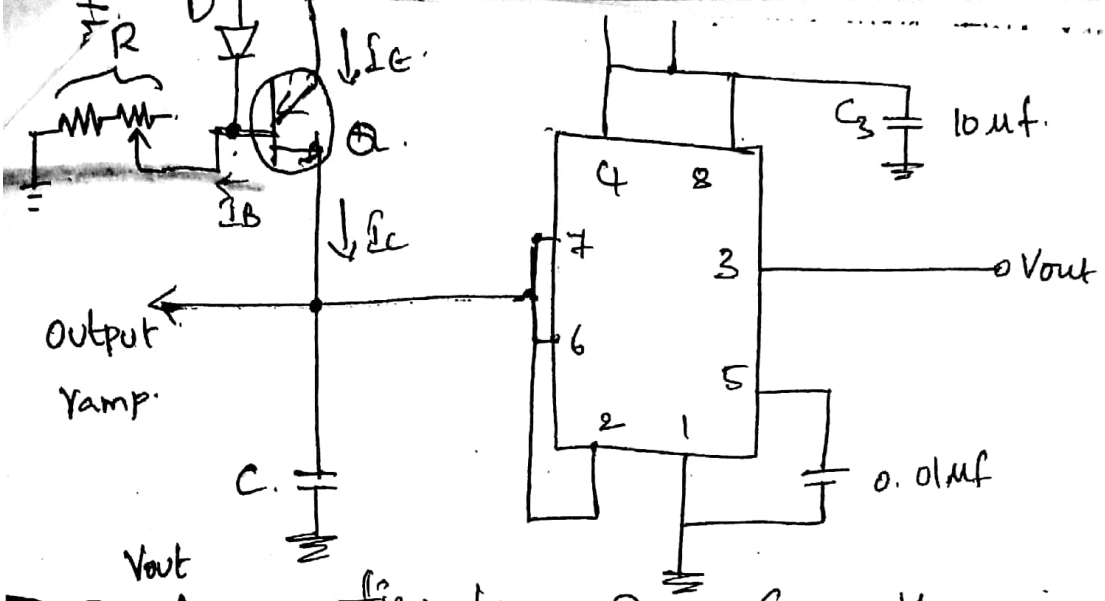


fig:- Linear Ramp Generator.

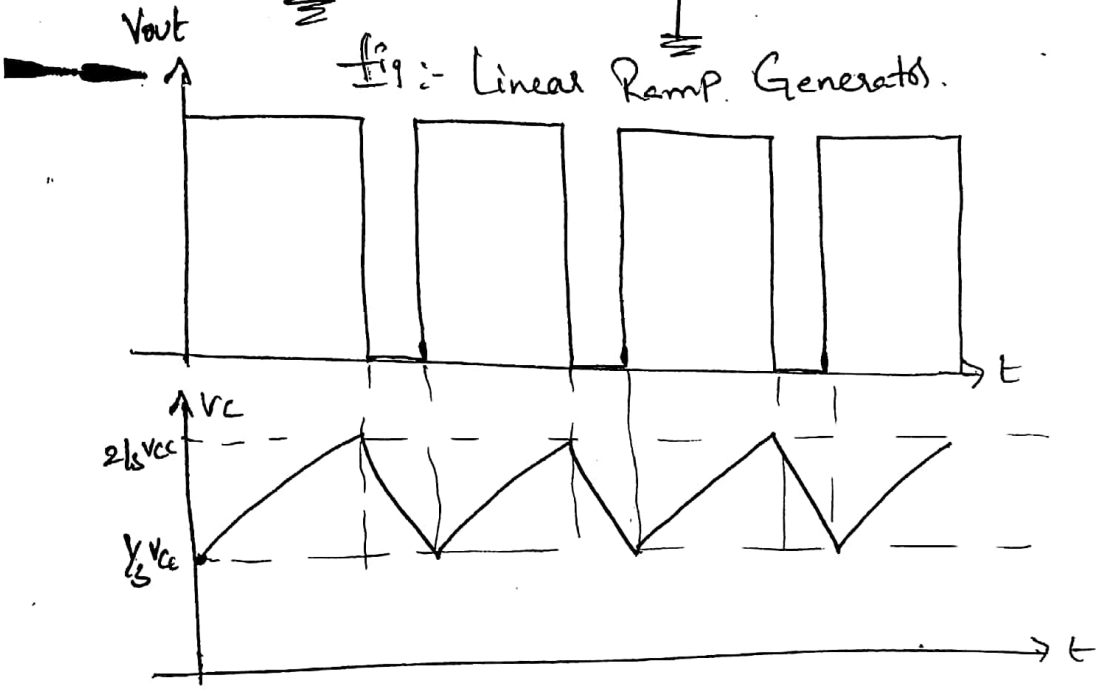


fig:- waveforms of ramp Generator

→ The ckt is used to obtain constant current I_C is a current mirror ckt, using transistor Q and diode 'D'. The current I_C, charges capacitor 'C' at a constant rate towards +Vcc. Capacitor voltage Vc becomes ($2/3 V_{cc}$) the Comparator makes internal transistor Q_1 ON within no time. But while discharging when Vc becomes ($1/3 V_{cc}$), the second Comparator makes Q_1 off and C starts its charing again. As discharging time of Capacitor 'C' is very small.

The time Period of Ramp is approximately given by

$$T = \frac{V_{cc} \cdot C}{3 I_C} \text{ sec}$$

where I_C = Charging Current = $\frac{V_{cc} - V_D}{R} = \frac{V_{cc} - V_{BE}}{R}$.

Hence $f = \frac{1}{T}$

$$f = \frac{3 I_C}{V_{cc} \cdot C} \text{ Hz}$$

Missing Pulse detector

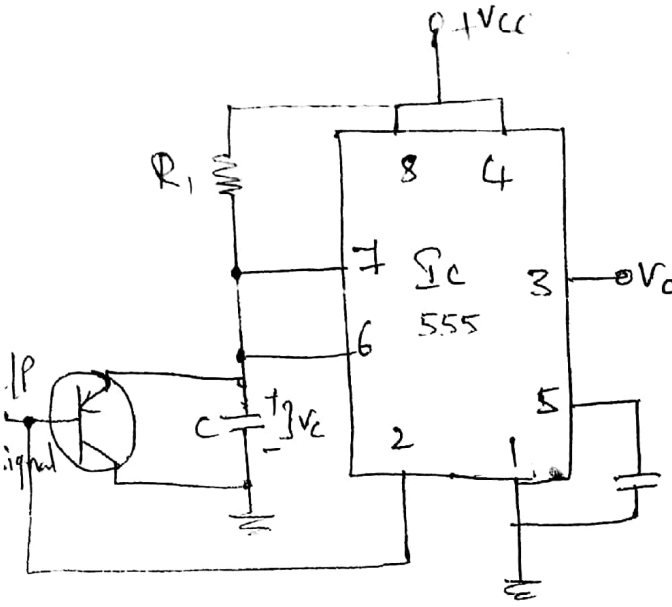


fig :- Missing Pulse detector

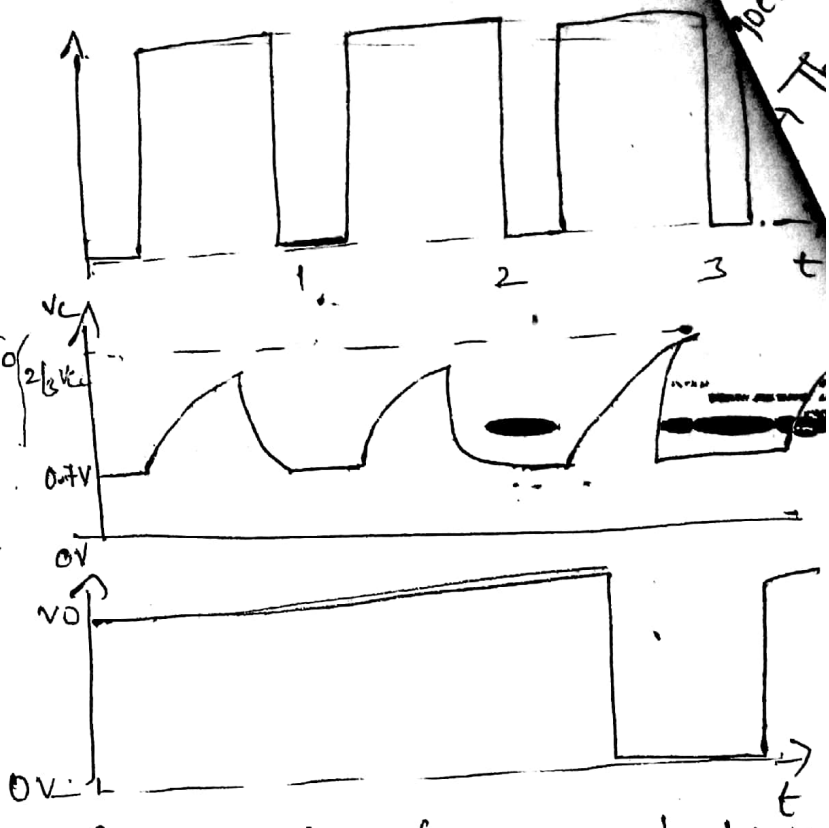


fig :- waveforms for missing pulse detector

→ for this Ckt timing interval is adjusted such that it is slightly longer than the Period of I/P signal. The Continuous low going pulses of the Period less than the timing interval do not allow Capacitor to Charge upto 2/3 Vcc. As a result, output voltage remains high. In Case of Missing Pulse (Pulse 3), Capacitor charges upto 2/3 Vcc. and forces o/p voltages into its low state. This type of Ckt Can be Used to detect a missing heart beat.

Pulse Position Modulation

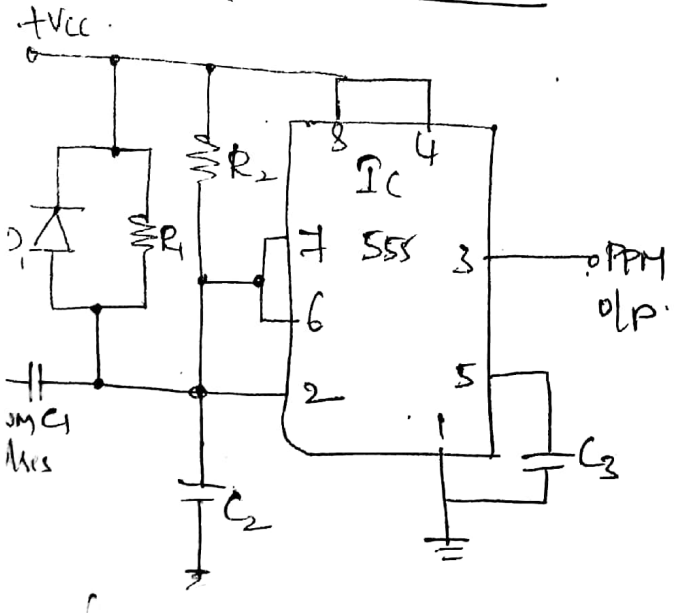


fig :- PPM generator
I/P

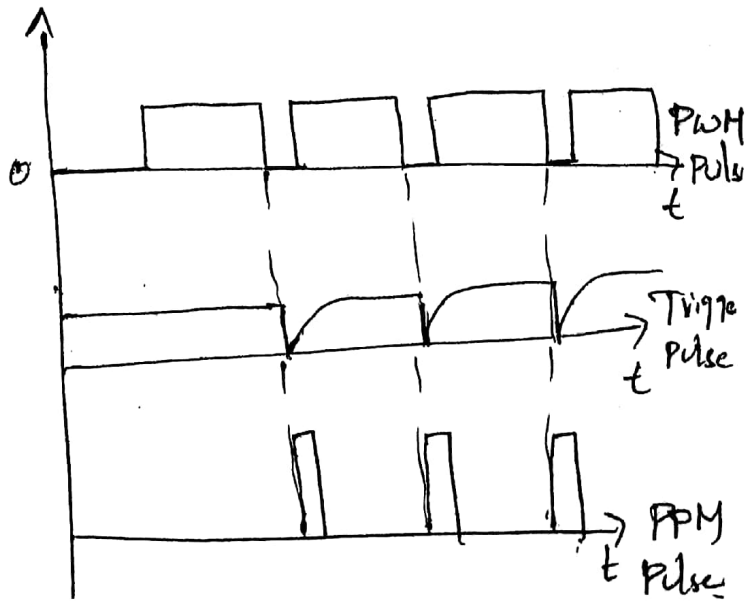


fig :- waveforms of PPM generator

goes low and $\bar{Q}$ goes high.

→ The low $\bar{Q}$ makes the transistor off. Thus Capacitor starts charging through the resistance R_A, R_B and V_{cc}. The charging Path is shown by thick arrow in the fig. As total resistance in the charging Path is $(R_A + R_B)$, the charging time Constant is $(R_A + R_B)C$.

→ Now the Capacitor voltage is also a threshold voltage. While charging Capacitor voltage increases. i.e the threshold voltage increases. When it exceeds $2/3\ V_{cc}$, then the Comparator 1 o/p goes high which sets the flip flop. o/p Q becomes high and o/p at Pin 3. i.e $\bar{Q}$ becomes low

→ High Q drives transistor Q_d in Saturation and Capacitor starts discharging through resistance R_B and transistor Q_d.

→ Thus the discharging time Constant is $R_B \cdot C$. When Capacitor voltage becomes less than $1/3\ V_{cc}$, Comparator 2 o/p goes high, resulting the flip flop. this cycle repeats.

→ Thus when Capacitor is charging, o/p is high while Capacitor is discharging o/p is low

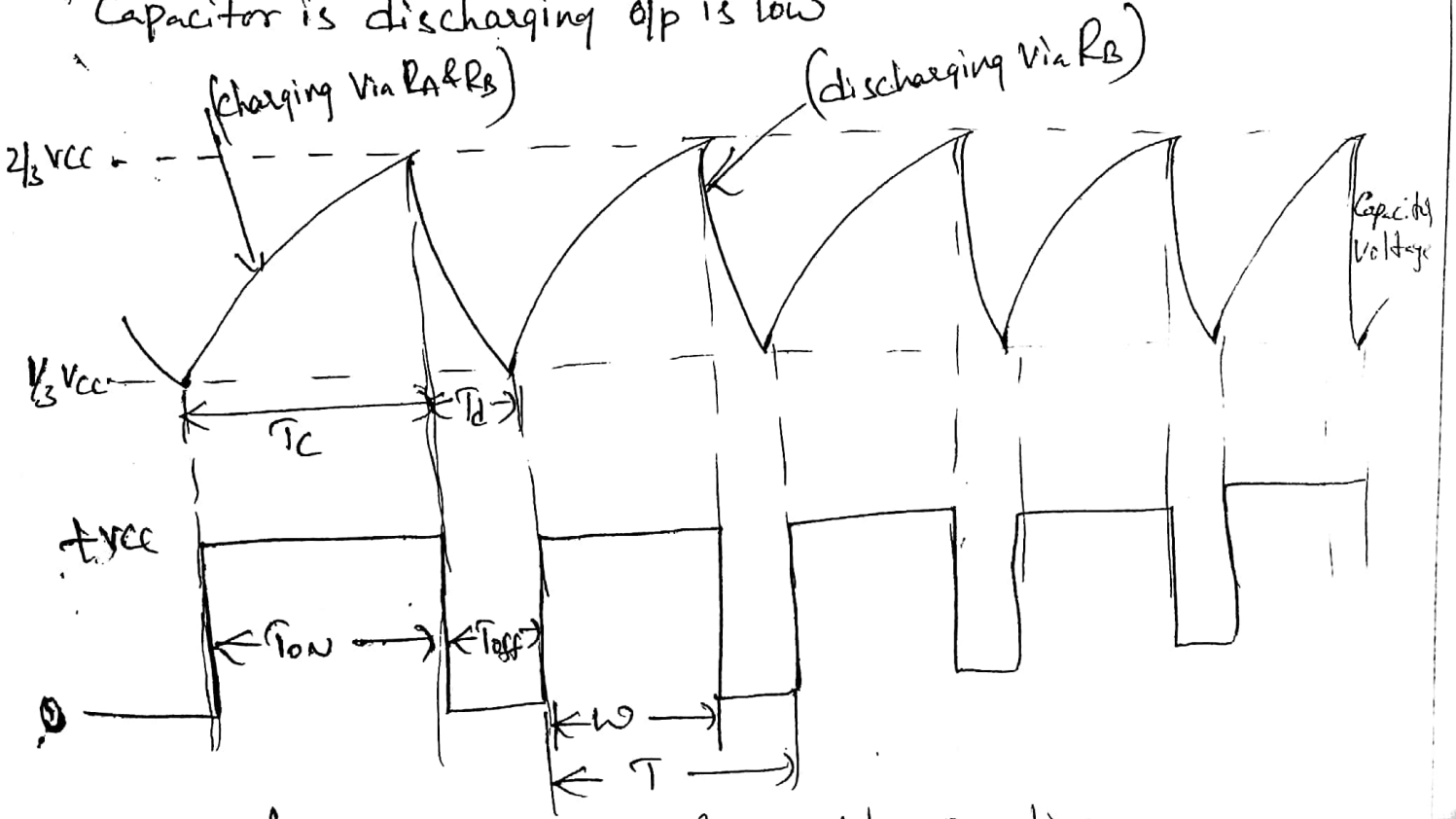


fig :- Waveforms of astable operation

Astable Multivibrator Using IC 555

The IC 555 Connected as an astable multivibrator. The thresh input is Connected to the trigger i/p. Two External resistances R_A, R_B is Used in the Circuit.

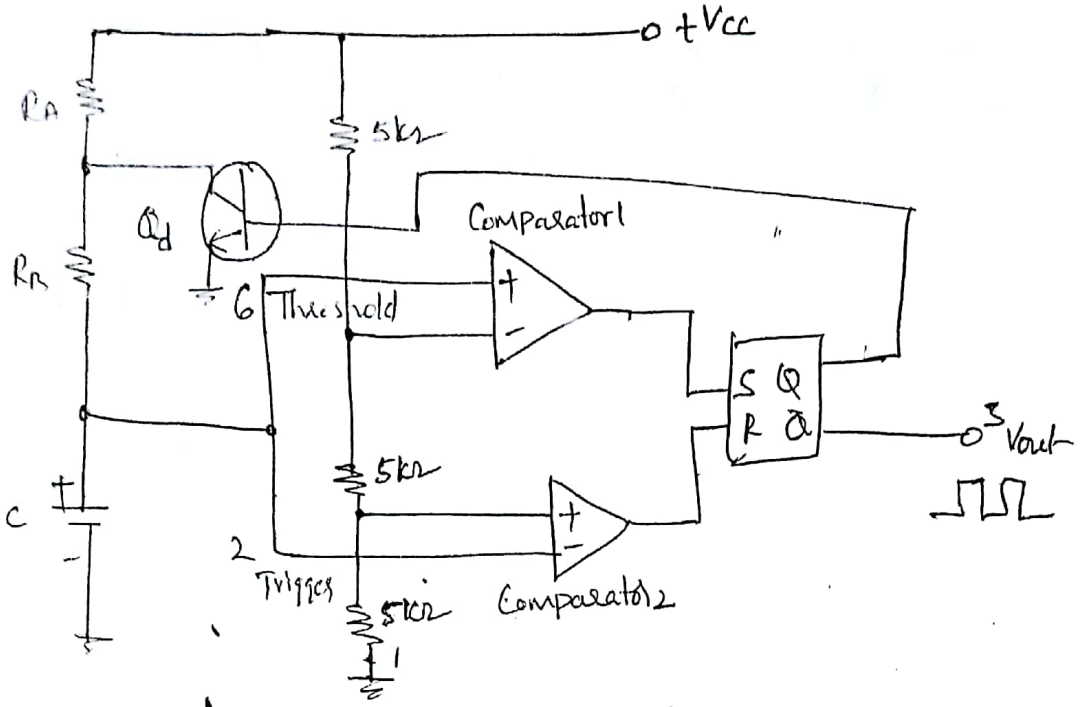


fig:- Astable Operation of 555.

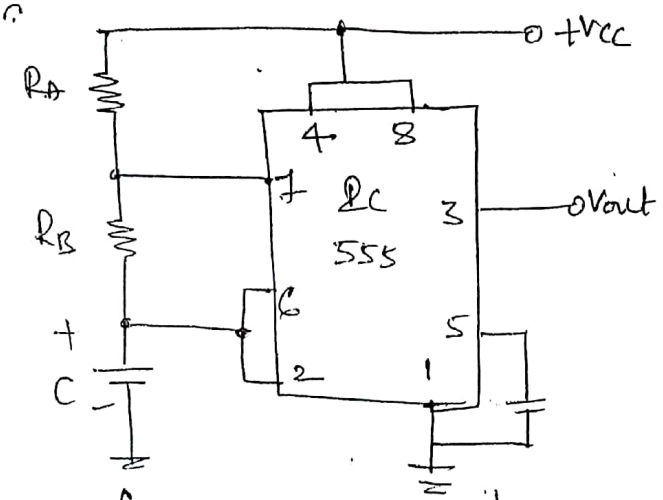


fig:- Schematic diagram.

→ This Circuit has no stable state. The ckt changes its state alternately. hence the operation is also Called free running nonsinusoidal oscillator.

Operation:-

→ When the flip-flop is Set, Q is high which drives the transistor Q_1 in Saturation and the Capacitor gets discharged. Now the Capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes

Duty Cycle :-

Generally the charging time Constant is greater than the discharg time Constant. Hence at the o/p, the waveform is not symmetric. The h o/p remains for longer Period than the low o/p.

→ The ratio of high o/p Period and low o/p Period is given by a mathematical Parameter Called duty cycle.

→ It is defined as the ratio of ON time i.e. high o/p to the total time of one cycle.

W = time for o/p is high = T_{ON}

T = time of one cycle

D = duty cycle = $\frac{W}{T}$

$$\%D = \frac{W}{T} \times 100\%$$

The charging time for the Capacitor is given by,

T_C = charging time = $0.693 (R_A + R_B) \cdot C$.

while the discharging time is given by

T_d = discharging time = $0.693 R_B \cdot C$

Hence the time for one cycle is

$$T = T_C + T_d = 0.693 (R_A + R_B) C + 0.693 R_B C.$$

$$T = 0.693 (R_A + 2R_B) C$$

$$W = T_C = 0.693 (R_A + R_B) C.$$

$$\%D = \frac{W}{T} \times 100 = \frac{0.693 (R_A + R_B) C}{0.693 (R_A + 2R_B) C} \times 100$$

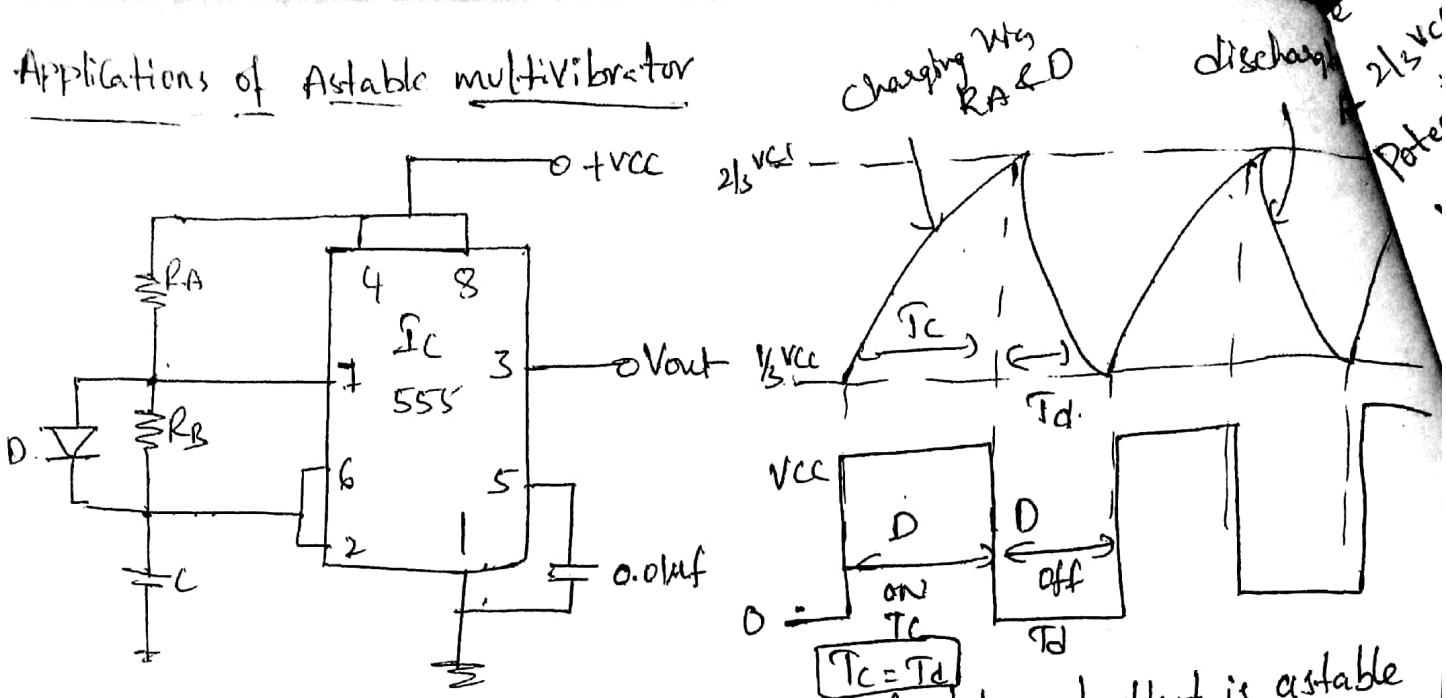
$$\%D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

while frequency of oscillation is given by

$$f = \frac{1}{T} = \frac{1}{0.693 (R_A + 2R_B) C}, \text{ i.e } f = \frac{1.44}{(R_A + 2R_B) C} \text{ Hz}$$

if R_A is much smaller than R_B, duty cycle approaches to 50% and o/p waveform approaches to Square wave.

Applications of Astable multivibrator



→ It can be observed from the expression of duty cycle that is astable operation exact 50% duty cycle is not possible to achieve.

→ To get Exactly 50% duty cycle i.e square wave o/p it is necessary to modify the astable times ckt.

→ In the modified ckt, the capacitor 'C' charges through R_A and diode D and discharges through R_B. To obtain square wave (50% duty cycle) resistance R_B is adjusted $\boxed{T_C = T_d}$

Voltage Controlled oscillator (VCO) :-

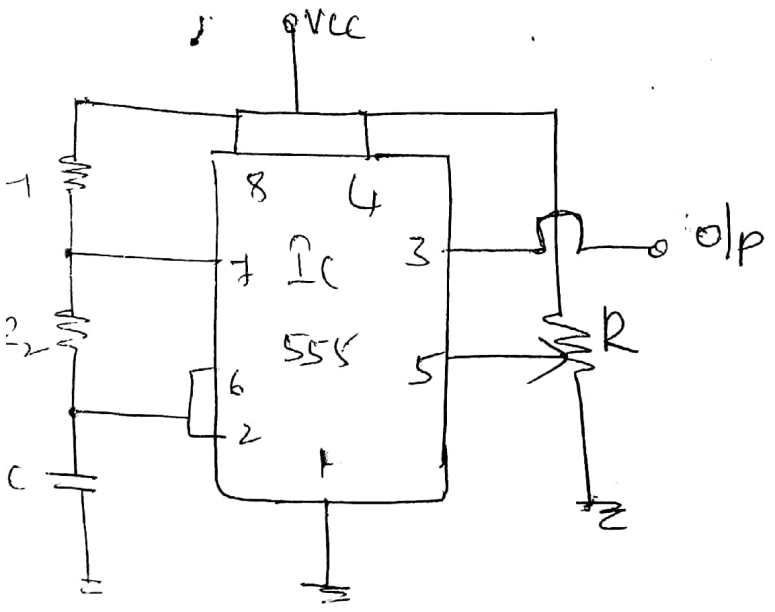


fig: VCO

We know that internally set voltage at the control voltage terminal is 2/3 Vcc. In this ckt, the Control Voltage is Externally set by the Potentiometer. With change in the Control Voltage, the upper threshold voltage changes and thus the time required to charge capacitor upto upper threshold voltage changes. Similarly, discharge time also changes. As a result, the frequency of the o/p voltage changes.

FSK Generator :-

Binary Code Consists of 1's and 0's. It can be transmitted by shift a Carrier frequency. one fin frequency represents one and other represent zero. This type of txion if Called FSK technique. Astable multivibrat Using 555 Can be used to generate fsk Signal

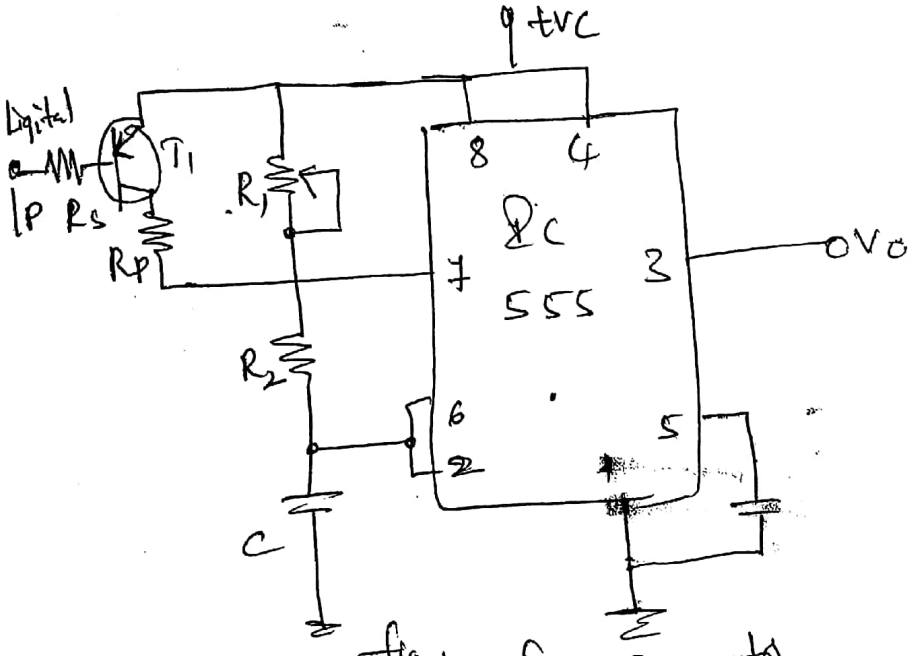


fig :- fsk Generator

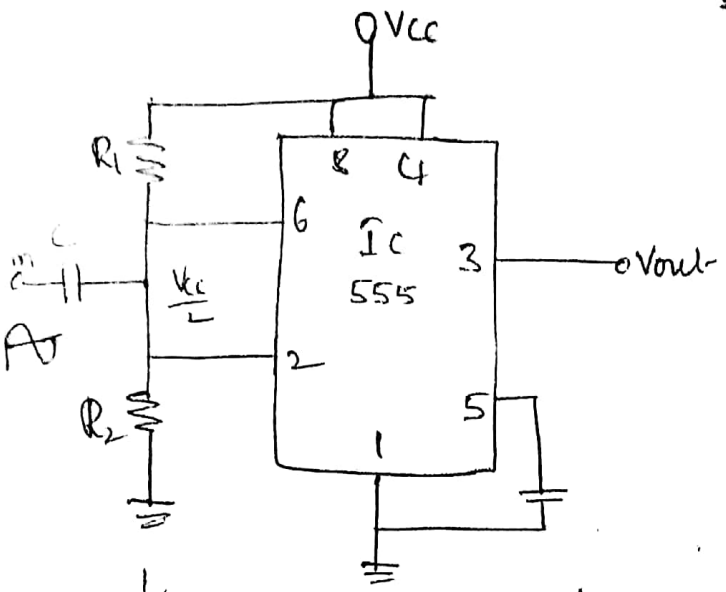
When digital i/p is HIGH (logic 1), transistor T_1 is off and 555 timer work in a normal astable mode

So $$f_o = \frac{1.45}{(R_1 + 2R_2)C}$$

When i/p is low., transistor T_1 is ON and Connects the resistance $R_1 \| R_p$

$$f_o = \frac{1.45}{[(R_1 \| R_p) + 2R_2]C}$$

Schmitt Trigger



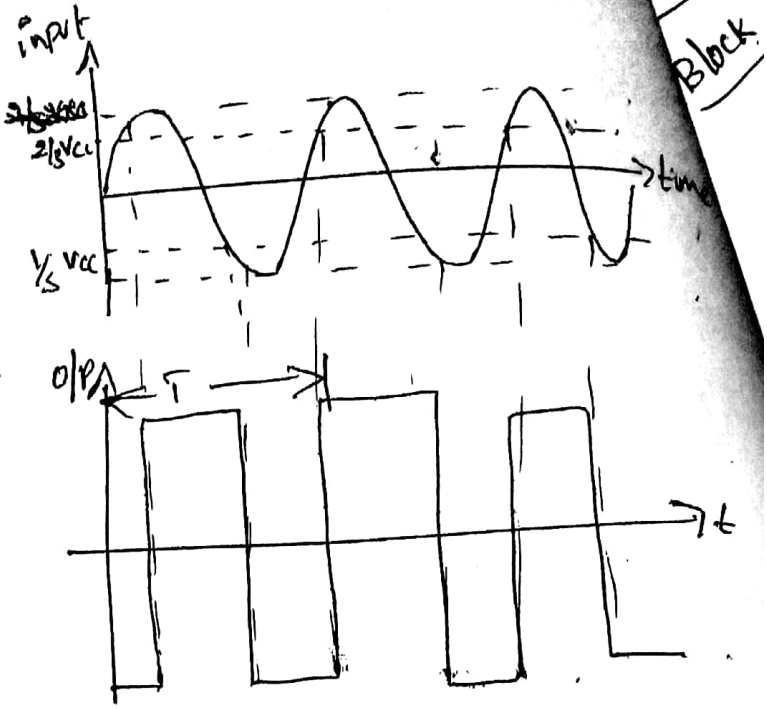


Fig:- 555 As a Schmitt Trigger

- 1) The i/p is given to the Pin 2 and 6 which are tied together. Pins 4 & 8 are connected to supply voltage +Vcc. The common Point of two Pins 2 and 6 is Externally biased at Vcc/2 through the resistance network R_1 & R_2. Generally $R_1 = R_2$ to get the biasing of Vcc/2. The upper Comparator will trip at 2/3 Vcc. while lower Comparator at 1/3 Vcc. The bias Provided by R_1 & R_2 is Centred within these two thresholds.
- 2) Thus when Sine wave of sufficient Amplitude, greater than Vcc/6 is applied to the ckt as i/p, it causes the internal flip flop to alternately set & Reset, due to this the ckt Produces the Square wave at the o/p

Comparision of Multivibrator Ckts.

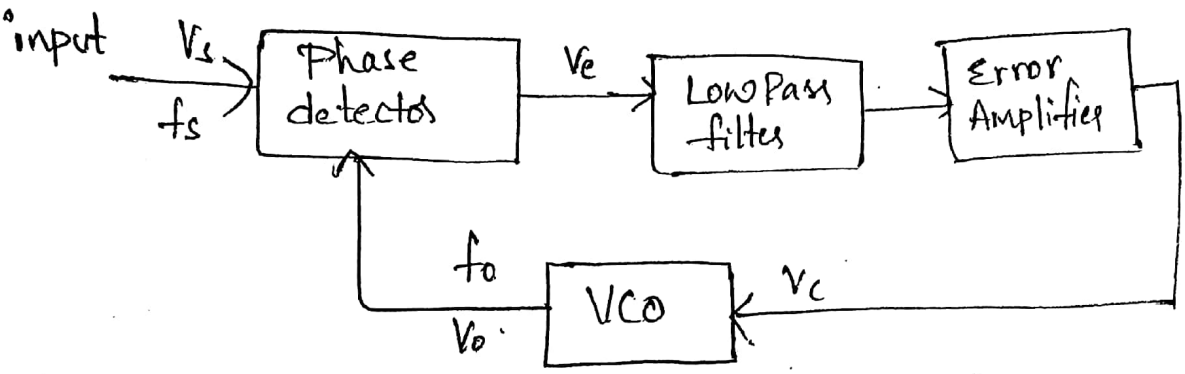
Monostable multivibrator	Astable multivibrator
1. It has only one stable state	1. There is no stable state
2. Trigger is required for operation to change the state.	2. Trigger is not required to change the state hence called free running oscillator
3. Two Components R & C are necessary with IC 555 to obtain the ckt	3. Three Components R_A, R_B & C are necessary with IC 555 to obtain the ckt.
4. The Pulse width is given by W = 1.1RC sec	4. The frequency is given by $f = \frac{1.44}{(R_A + 2R_B)}$ Hz
5. The freq of operation can be controlled by freq of trigger Pulses applied	5. The freq of operation is Controlled by R_A, R_B & C
6. The astable can also be used as frequency divider,	6. The application are Square wave generator

Phase locked Loop (PLL) :-

Block diagram of Phase locked loop :-

The main blocks of Phased lock loop are

1. Phase detector (or) Comparator.
2. Low Pass filter.
3. Error Amplifier
4. Voltage Control oscillator (VCO).



1. Voltage Controlled oscillator (VCO) :- The VCO is a free running multi-vibrator and operates at a set frequency fo called free running frequency. This frequency is determined by an external timing capacitor and an external resistor It can also be shifted to either side by applying a dc Control voltage Vc to an appropriate terminal of the IC.

→ The frequency deviation is directly Proportional to the dc control voltage and hence it is called a voltage Controlled oscillator (or) VCO.

2. Phase detector :- If an i/p signal Vs of frequency fs is applied to the PLL the phase detector Compares the phase and frequency of the incoming signal to that of the o/p Vo of the VCO. If the 2 signals differ in frequency and/or phase an error voltage. Ve is grounded

3. Low Pass filter :- The o/p of the Phase detector Contains Sum (fs+fo) and difference (fs-fo) Components. The high frequency Components (fs+fo) is removed by the Low Pass filter and Produces the difference frequency Components (fs-fo).

4. Error Amplifier :- The difference frequency Component is amplified by the Error amplifier and then applied as Control voltage Vc to VCO.

5. VCO :- The Signal Vc shifts the VCO frequency in a direction to reduce the frequency difference b/w fs & fo. Once this action starts we say that the Signal is in the Capture range.

→ The VCO Continuous to change frequency till its o/p frequency is Exactly Same as the i/p Signal frequency the ckt then said to be locked.

→ Once locked PLL tracks the frequency changes of the i/p Signal.

1. free running.
2. Capture
3. locked (or) Tracking.

Important definitions Related to PLL

Lock Range :- The Range of frequencies over which the PLL Can maintain lock with the incoming Signal is Called lock range (or) Tracking range.

Capture Range :- The range of frequencies over which the PLL Can acquire lock with an i/p Signal is Called the Capture range.

Pull-in-time :- The total time taken by the PLL to Establish a lock is Called Pull-in-time.

11) Phase detector :-

There are two types of Phase detectors

1. Analog
2. Digital.

Analog phase detector

There are two types of Analog Phase detectors

1. Switch type
2. Balanced modulator type.

Type 1 Phase detector:-

It consists of electronic switch, S. The switch is opened and closed by signal coming from VCO

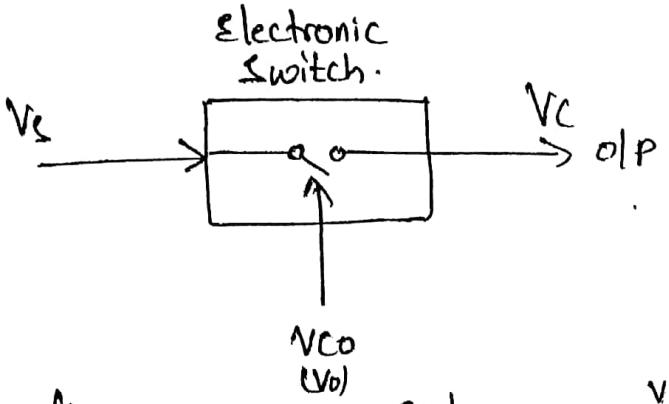


fig:- VCO Basic Ckt.

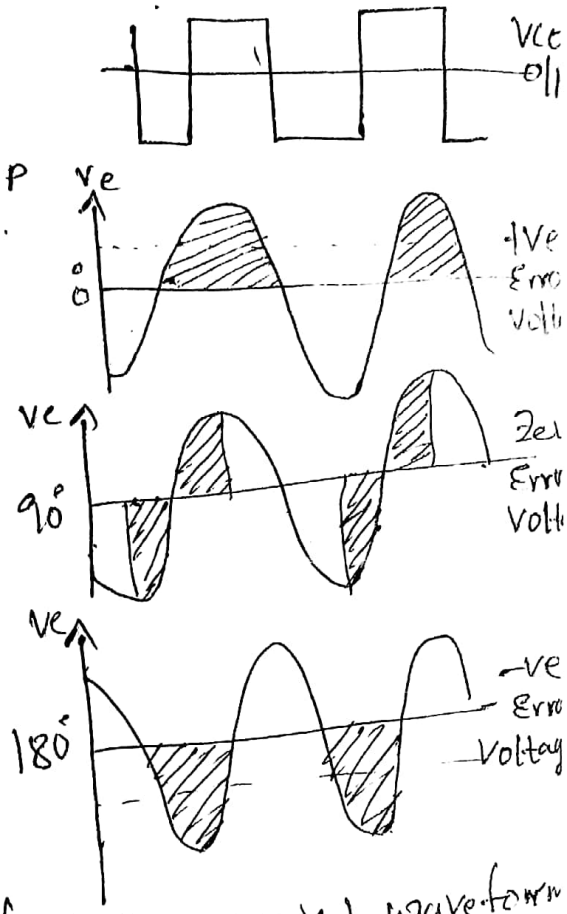


fig:- Typical waveforms

→ Assuming that the signal from VCO operates the electronic switch, the i/p sinusoid v_i is chopped by the VCO frequency.

→ The o/p of the phase detector when passed through the filter gives out an average error signal shown as dotted line.

→ The error voltage is zero when the phase difference blw the two i/p's equals 90°. The error voltage is positive for a phase difference of 0° and -ve for a phase difference of 180°.

→ The PLL achieves a perfect lock when VCO o/p is in phase (or) 90° out of phase with the i/p.

Considering the i/p signal $v_i = V_i \sin \omega_i t$

VCO o/p $v_o = V_o \sin(\omega_o t + \phi)$

The phase detector o/p V_e becomes

$$V_e = K V_i V_o \sin(\omega_i t) \sin(\omega_o t + \phi)$$

where K is the gain of the phase comparator and ϕ is the phase difference blw i/p signal v_i and VCO o/p v_o, then

$$V_e = \frac{K V_i V_o}{2} \left[\cos(\omega_i t - \omega_o t - \phi) - \cos(\omega_i t + \omega_o t + \phi)\right]$$

when locked $\omega = \omega_o$

hence, $$V_e = \frac{K V_i V_o}{2} \left[\cos(-\phi) - \cos(2\omega_o t + \phi)\right]$$

The double frequency term is eliminated by Lpf and the dc error vo due to the term Cos ϕ. It can be observed that when $\phi = 90°$, Perfect lock achieved and hence the error voltage $V_e = 0$. from the above eqn, it is clea that the o/p error voltage V_e is dependent on.

i) The i/p signal amplitude V_i, which makes the phase detector gain and loop gain also dependent on V_i

ii) Cos ϕ, that makes the response non-linear.

Balanced modulator type phase detector

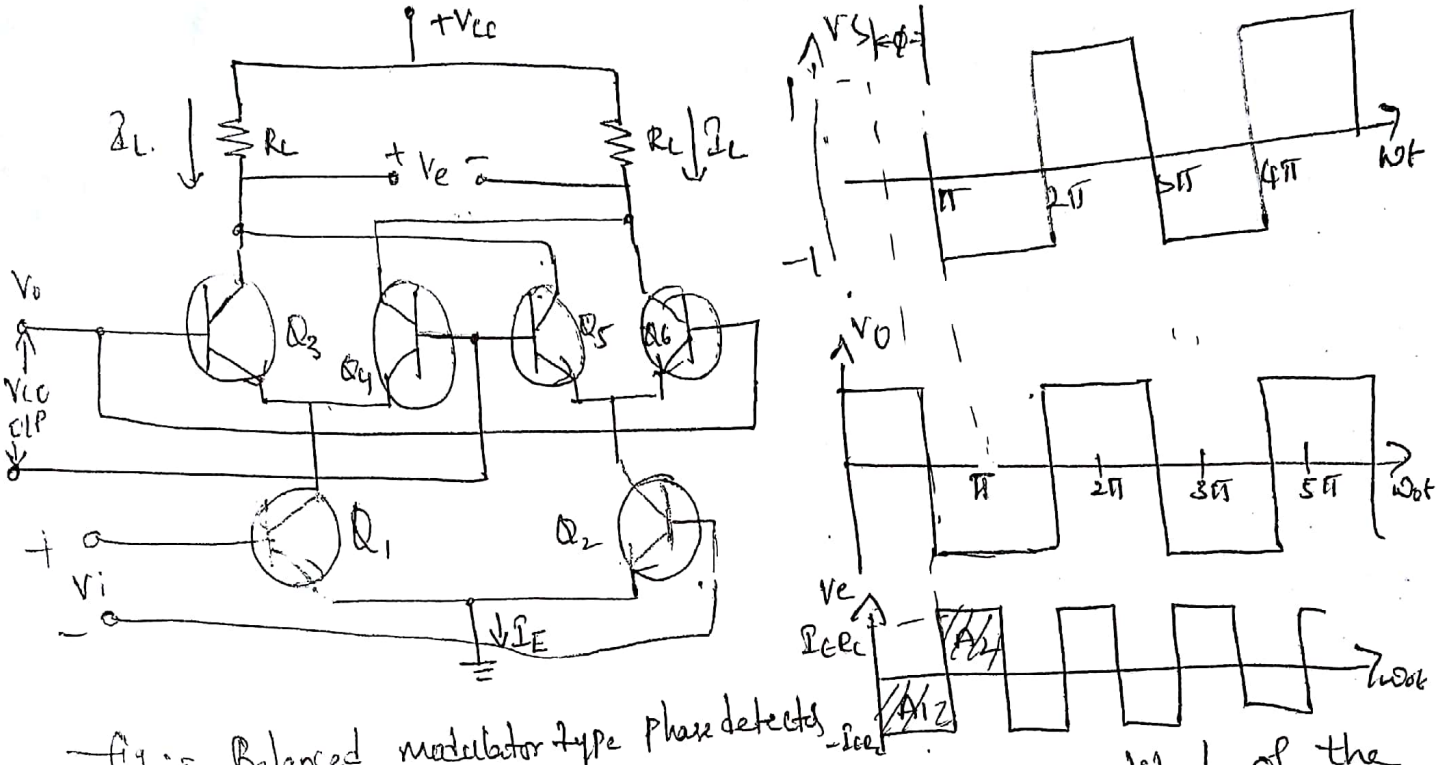


Fig :- Balanced modulator type phase detector

The above Problems can be eliminated by making amplitude of the input signal Constant. This can be achieved by Converting sinusoidal input signal into square wave input signal.

- The waveforms for balanced modulator type phase detector with phase shift of ϕ b/w i/p signal and the VCO op signal. When V_s is +ve Q_1 is ON and Q_2 is off.
- when V_o is +ve Q_3 and Q_6 are ON, and Q_4 and Q_5 are off.
- Obviously, when V_s is -ve Q_1 is off and Q_2 is ON. Similarly, when [illegible] off and Q_4 & Q_5 are ON. These Conditions

The o/p error voltage is given by

$$V_e = I_E R_L$$

The average value of the o/p voltage of the phase detector, V_e can be obtained as $V_{e(av)} = \frac{1}{\pi}(a_1 + a_2)$

where a_1 = shaded area in the -ve half

a_2 = " " " " +ve "

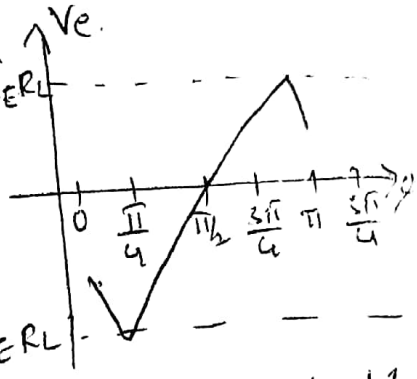


fig:- relationship b/w V_e & ϕ

$$V_{e(av)} = \frac{1}{\pi}\left[(-I_E R_L)(\pi - \phi) + (I_E R_L)(\phi)\right]$$

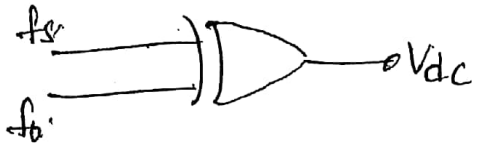
$$= \frac{I_E R_L}{\pi}\left[-\pi + \phi + \phi\right] = \frac{2 I_E R_L}{\pi}\left[\phi - \frac{\pi}{2}\right]$$

$$V_{e(av)} = \frac{4 I_L R_L}{\pi}\left[\phi - \frac{\pi}{2}\right] \quad \because I_E = 2 I_L.$$

$$\boxed{V_{e(av)} = K\phi\left[\phi - \frac{\pi}{2}\right]}$$ where $K\phi = \frac{4 I_L R_L}{\pi}$

Digital Phase detector

i) Phase detector using XOR gate



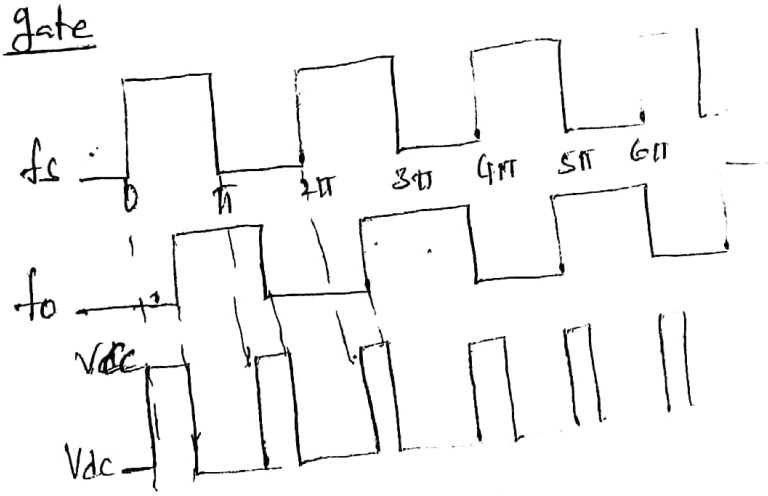


fig i/p and o/p waveforms

→ The XOR gate can be used as a digital phase detector when both signals fs and fo are square waves. This we know that the o/p of XOR gate is high when only one of the i/p signals is high. The input and output waveforms for digital phase detector. Here, fs is leading fo by ϕ degrees

$$K\phi = \frac{V_{cc}}{\pi} \quad \text{for } V_{cc} = 5V, \quad K\phi = \frac{5}{\pi} = 1.591 \text{ V/rad.}$$

Phase detector using RS flip-flop

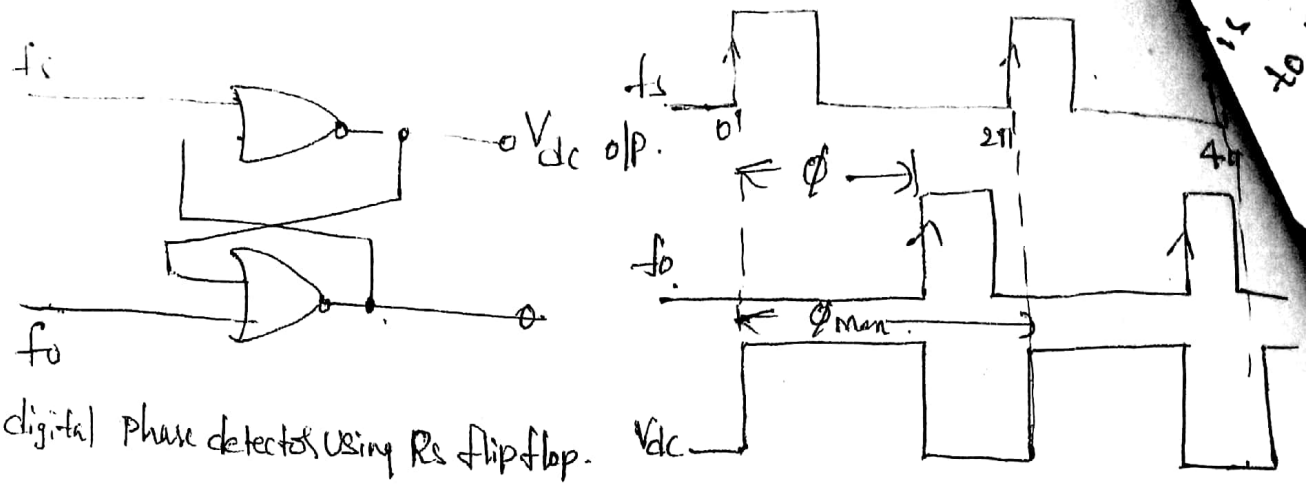


fig:- digital phase detector using Rs flipflop.

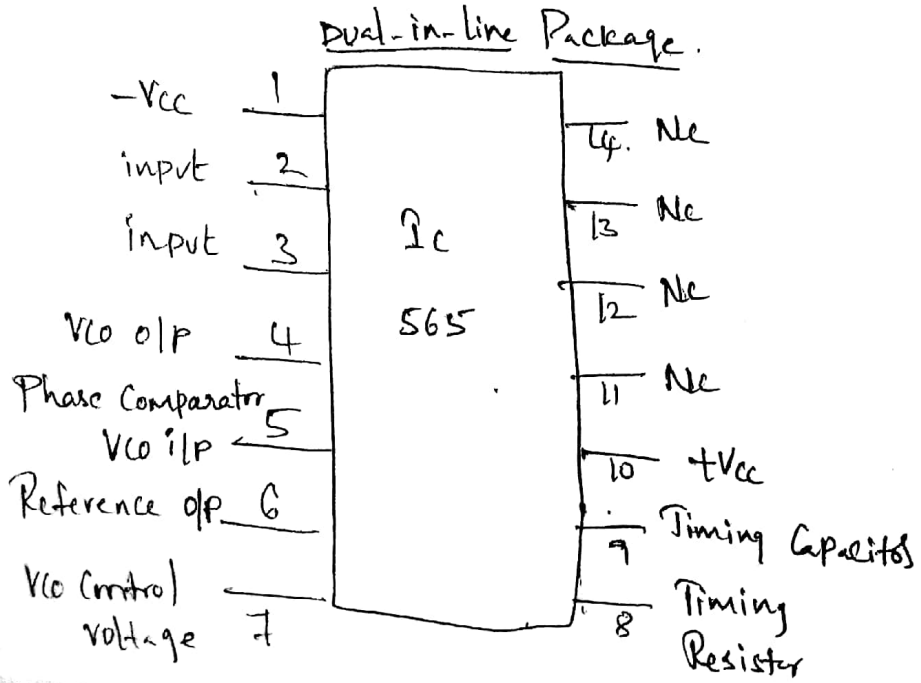
→ The digital phase detector using edge-triggered Rs flip flop. This phase detector is used when fs & fo are both pulse waveforms with duty cycle less than 50%.

→ The flip flop consists of NOR gates and it changes its state at the +ve edge going

→ The rising edge of the i/p signal, o/p goes high and at the rising edge of the VCO o/p signal, o/p goes low. Since the duty cycle of signals is less 50%. max ϕ can approach upto 360°

Monolithic phase locked loop IC 565

Dual-in-line Package.



i/p

Block diagram of IC 565 PLL consists of Phase detector, amplifier, LPF and VCO. As shown in the block diagram the phase locked feedback loop is not internally connected. Therefore, it is necessary to connect o/p of VCO (Pin 4) to the phase comparator input (Pin 5), Externally. In frequency multiplication applications a digital frequency divider is inserted into the loop i.e btw Pin 4 and Pin 5.

→ The centre frequency of the PLL is determined by the free running freq of the VCO and it is given by

$$f_0 = \frac{1.2}{4R_1C_1} \text{ Hz}$$

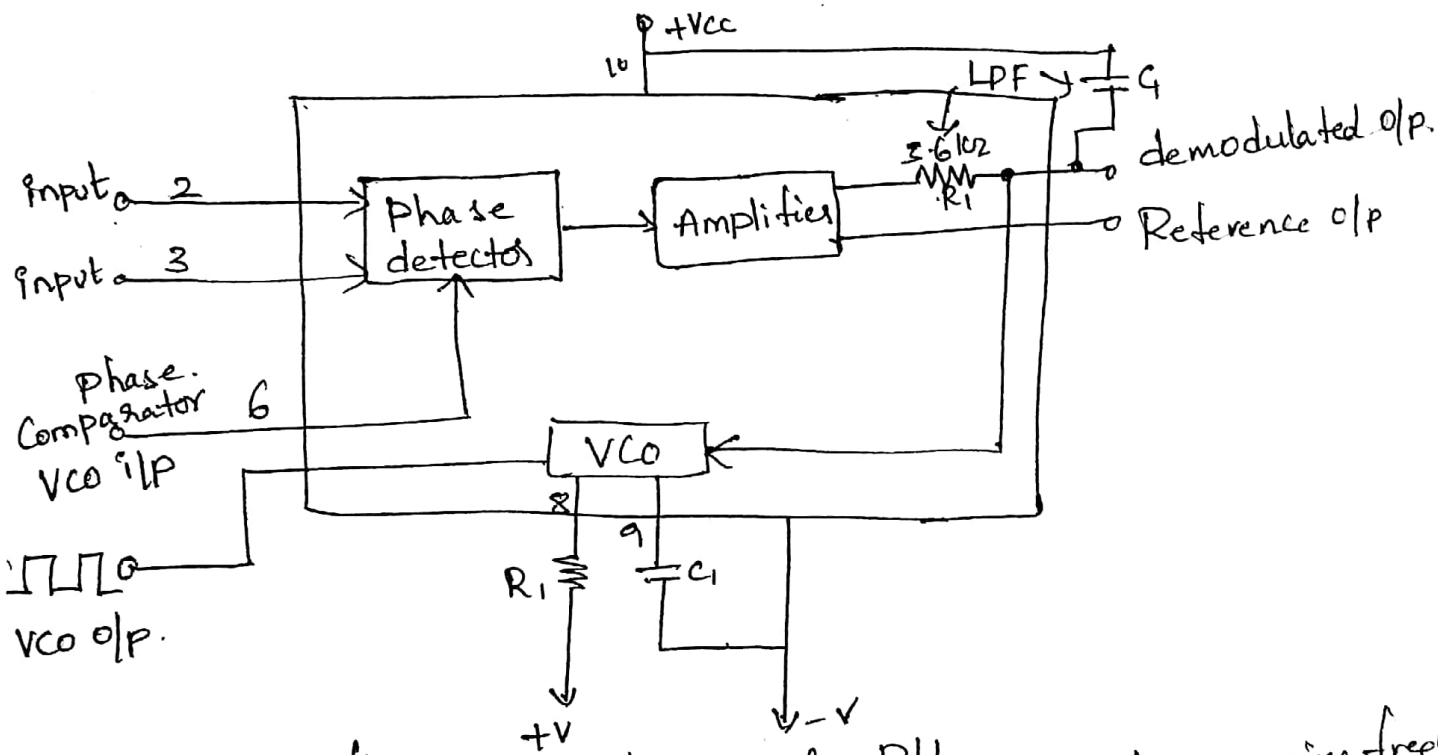


fig :- Block diagram of PLL.

→ The values of R_1 & C_1 are adjusted such that the free running frequency will be at the centre of the i/p frequency range. The value of Capacitor C_2 should be large Enough to Eliminate Possible oscillations in the VCO voltage

The lock range is given by $f_L = \pm \frac{8f_0}{V}$ Hz

where f_0 = free running freq of VCO in Hz

$V = (+V) - (-V)$ volts.

The Capture range is given by $f_C = \pm \left[\frac{f_L}{2\pi(3.6)(10^3)C_2}\right]^{1/2}$

Derivation of lock Range :-

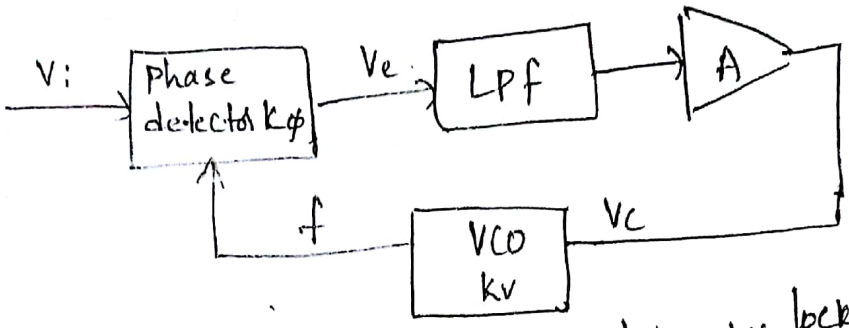


fig :- Block diagram to determine lock-range

let us assume that the o/p voltage of the phase detector is

$$V_e = K_\phi(\phi_e - \pi/2) \quad \text{where } \phi_e = \text{Phase Error.}$$

The o/p voltage of the phase detector is filtered by the low Pass filter to remove the high freq. Components. The o/p of the filter is amplified by a gain A and. then applied as the Control voltage V_c to the VCO as given by.

$$V_c = A V_e = K_\phi A (\phi_e - \pi/2). \quad \text{---(1)}$$

This Control voltage V_c will result in a shift in the VCO frequency from its Centre freq f_o to a freq f, given by.

$$f = f_o + K_v V_c \quad \text{---(2)}$$

When the PLL is locked in to the i/p Signal freq f_i, we have

$$f = f_i = f_o + K_v \cdot V_c \quad \text{---(3)}$$

Sub value V_c from Eq^n (3) we have

$$f_i - f_o = K_v \cdot K_\phi A (\phi_e - \pi/2)$$

$$\phi_e - \pi/2 = \frac{f_i - f_o}{K_v K_\phi A}$$

$$\phi_e = \frac{f_i - f_o}{K_v K_\phi A} + \frac{\pi}{2}$$

The max o/p voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radians and is

$$V_e(max) = \pm K_\phi(\pi/2)$$

The Corresponding value of the maximum Control voltage available to drive the VCO will be

$$V_c(max) = \pm K_\phi(\pi/2) A.$$

$f_i - f_o = K_v K_\phi (\pi/2) A$

$f_i = f_o \pm K_v K_\phi (\pi/2) A$

$f_i = f_o \pm \Delta f_L$

where $2\Delta f_L$ will be lock. in freq range given by

lock range $= 2\Delta f_L = K_v K_\phi A \pi$ $\quad \therefore \Delta f_L = K_v K_\phi A \pi/2$.

The lock in range is symmetrically located with respect to VCO free running freq f_o, for PLL565

$K_v = \frac{8 f_o}{V}$, $K_\phi = \frac{1.4}{\pi}$

$V = +V_{cc} - (-V_{cc})$ $\quad A = 1.4$.

So, $\Delta f_L = \frac{8 f_o}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2}$

$$\boxed{\Delta f_L = \pm \frac{7.84 f_o}{V}}$$

Derivation of Capture range :-

The Capture range is the range of i/p frequencies for which the initially unlocked loop will lock on an i/p signal. This is always less than the lock range.

→ When PLL is not locked the phase angle difference between the signal and the VCO o/p voltage is given by.

$$\phi_e = (\omega_s t + \theta_s) - (\omega_o t + \theta_o)$$

$$\phi_e = (\omega_s - \omega_o) t + \Delta\theta$$

The phase angle difference thus not be constant, but will change with time at a rate given by

$$\frac{d\phi_e}{dt} = \omega_s - \omega_o$$

The Phase detector o/p voltage will therefore not have a dc Compone... rather will have an Ac voltage with a triangular waveform of Peak ampl... $K\phi(\pi/2)$ and the fundamental freq of $\omega_s - \omega_o$ i.e $f_s - f_o = \Delta f$.

Let us derive an approximate expression for capture range for PLL emplo... a simple lag filter. The transfer function a simple lag filter is given by.

$$F(j\omega) = \frac{1}{1+j\omega T_1} = \frac{1}{1+j\left(\frac{\omega}{\omega_1}\right)} = \frac{1}{1+j\left(\frac{f}{f_1}\right)}$$

$$T_1 = RC, \quad \omega_1 = \frac{1}{RC}$$

$$F(f) = \frac{1}{1+j\,|f|f_1)}$$

$\therefore (f/f_1)^2 \gg 1.$

So $$F(f) = \frac{1}{j(f/f_1)} = \frac{f_1}{jf}$$

$$F(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{f_s - f_o}$$

The voltage available to drive the vco is given by

$$V_c = V_e \times F(\Delta f) \times A$$

(or) $$V_c = V_{e(max)} \times F(\Delta f) \times A$$

$$V_c = \pm K\phi(\pi/2) \times f_1/\Delta f \times A$$

The corresponding value of the max freq shift will be

$$(f - f_o)_{max} = K_v V_{c(max)}$$

$$(f - f_o)_{max} = \pm K_v K\phi(\pi/2) A\left(\frac{f_1}{\Delta f}\right).$$

Since $\Delta f_{cap} = (f - f_o)_{max}$ we have.

$$\Delta f_{cap} = \pm K_v K\phi(\pi/2) A \frac{f_1}{\Delta f_{cap}}$$

$$(\Delta f_{cap})^2 = \pm K_v K\phi A \pi/2 f_1$$

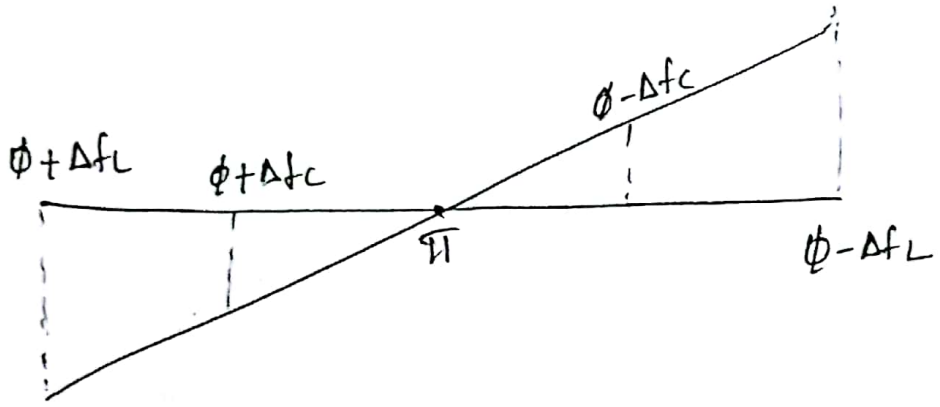
$$|\Delta f_{cap})^2 = \pm \Delta f_L \cdot f_1$$

$$\Delta f_{cap} = \pm \left[\frac{\Delta f_L}{2\pi RC} \right]$$

for IC PLL 565, R = 3.6 kΩ

$$\Delta f_{cap} = \pm \left[\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C} \right]^{V_2}$$

The total capture range is $2\Delta f_{cap}$.



Applications of PLL :-

1) Frequency multiplier :-

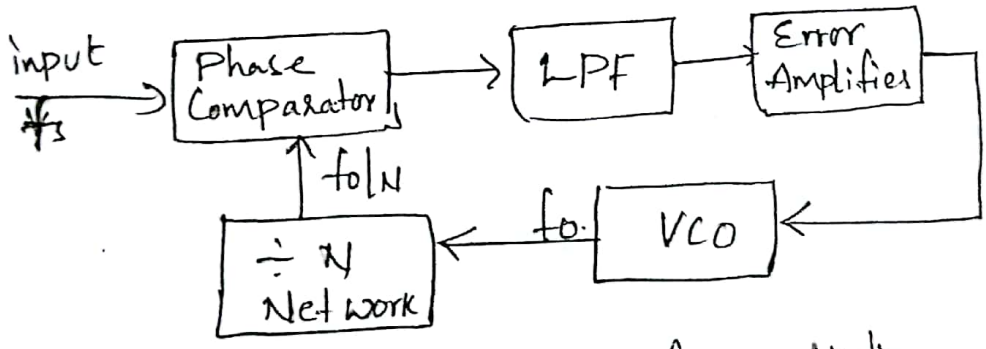


fig :- Block diagram of freq multiplier.

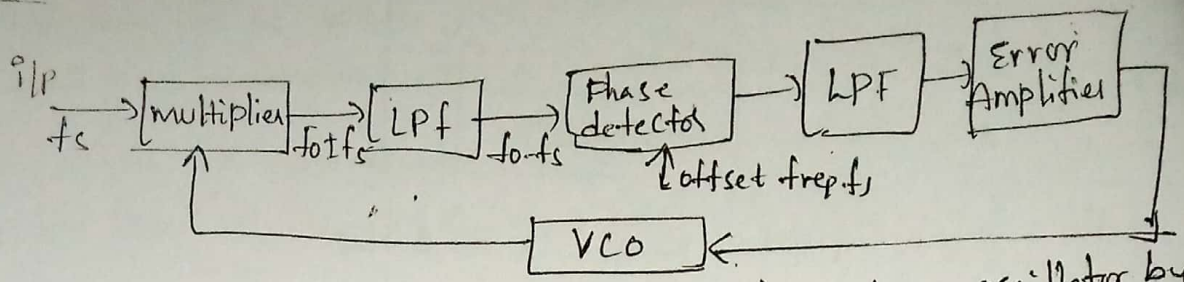
→ Here a divide by N Network is inserted b/w the VCO o/p and the Phase Comparator i/p. Since the o/p of the divider is locked to the i/p freq f_i, the VCO is actually running at a multiple of the i/p freq.

∴ in the locked state, the VCO o/p freq f_o is given by

$$f_o = N f_i$$

→ By selecting Proper divider by N N/W, we can obtain desired multiplication.

Frequency Translation



-) The freq translation means shifting the freq of an oscillator by a small factor.

→ It consists of mixer, low Pass filter and the PLL. The i/p freq f_s which has to be shifted is applied to the mixer. Another i/p to the mixer is the o/p voltage of VCO f_o.

→ The o/p of mixer contains the sum & difference signal $(f_o \pm f_s)$. The low pass filter connected at the o/p of mixer rejects the $(f_o + f_s)$ signal and gives only $(f_o - f_s)$ signal at the o/p.

→ The $(f_o - f_s)$ signal is applied to the phase detector. Another input to phase detector is the offset freq f_1.

$$f_o - f_s = f_1 \text{ and}$$

$$f_o = f_s + f_1$$

By adjusting offset freq f_1 we can shift the freq of the oscill. for to the desired value.

AM Detection :

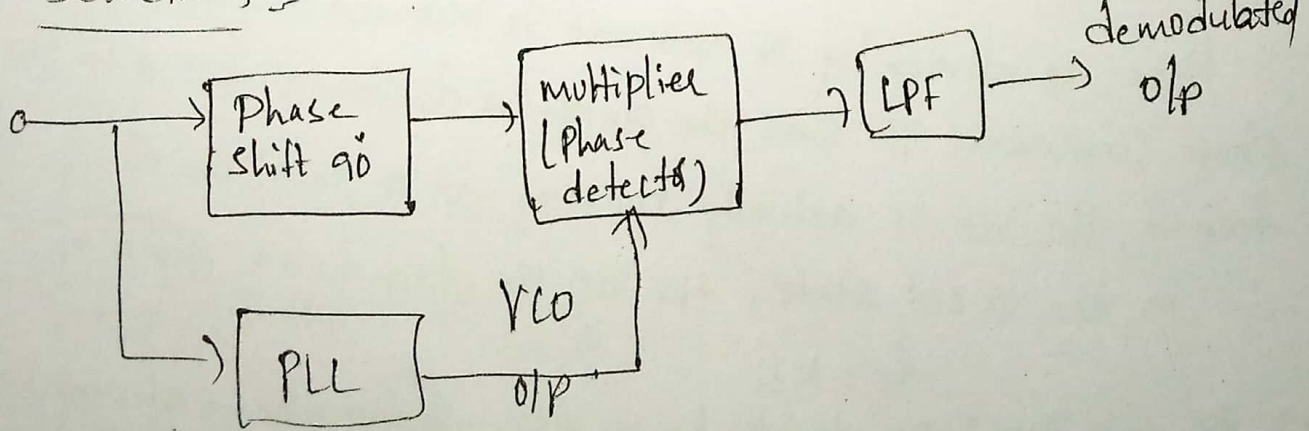


fig:- PLL Used as AM demodulator.

Modulated signal with 90 phase shift and the unmodulated from o/p of PLL are fed to the multipliers. Since VCO op is always 90 out of phase with the incoming AM signal under the locked condition, both the signals applied to the multipliers are in same phase.

→ The o/p of the multipliers contains both the sum and difference signals the low pass filter rejects high freq components. gives demodulated o/p.

FM Demodulator:-

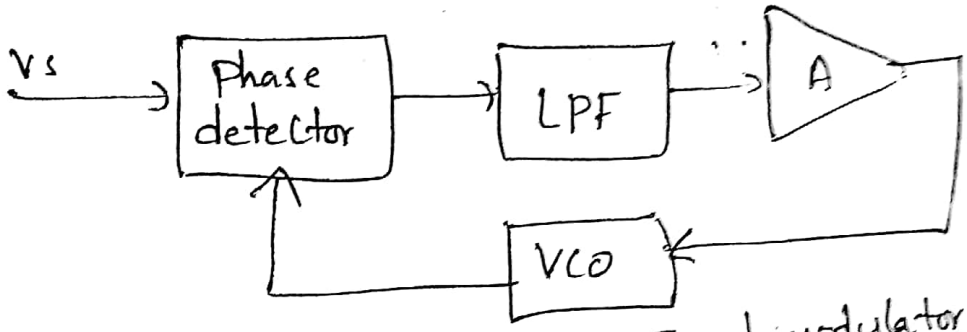


fig:- PLL as a FM demodulator

→ when the PLL is locked in on the fm signal, the VCO freq allows the instantaneous freq of the FM signal, and the error voltage (or) VCO control voltage is proportional to the deviation of the i/p freq from the centre frequency.

Frequency shift keying demodulator (FSK)

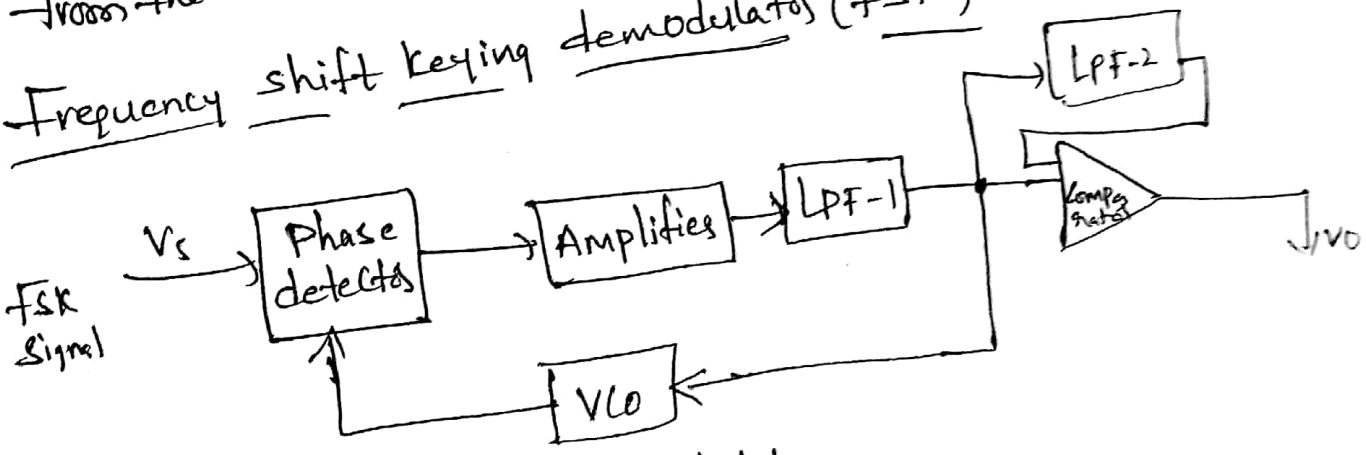


fig:- FSK demodulator.

→ A PLL can be used as a fsk demodulator. It is similar to the PLL demodulator for analog FM signals except for the addition of a comparator to produce a reconstructed digital o/p signal